CHAPTER 8

Driving Transistors and Thyristors

The thyristor, being a multiple (three) bipolar junction device, is essentially a current-controlled device. As illustrated in figure 8.1a, a current must be supplied between the gate and cathode terminals to produce cathode injection, hence anode current flow, provided the anode is forward biased. The magnitude of gate drive current determines the delay time and the anode current rise time. In gate commutated thyristors, a negative gate current must be produced, the magnitude determining the turn-off delay time and anode current fall time.

The power MOSFET and IGBT are voltage controlled devices with turn-on and turn-off requirements fundamentally different to bipolar devices. With the n-channel enhancement-mode power MOSFET and IGBT, a positive voltage must be applied between the gate and source terminals to enhance a channel which allows a drain current, if the drain is positively biased with respect to the source, as shown in figure 8.1b. Generally the MOSFET and IGBT are easier to drive than the bipolar thyristor, and only a few basic considerations are required for MOSFET and IGBT gate circuit implementation.

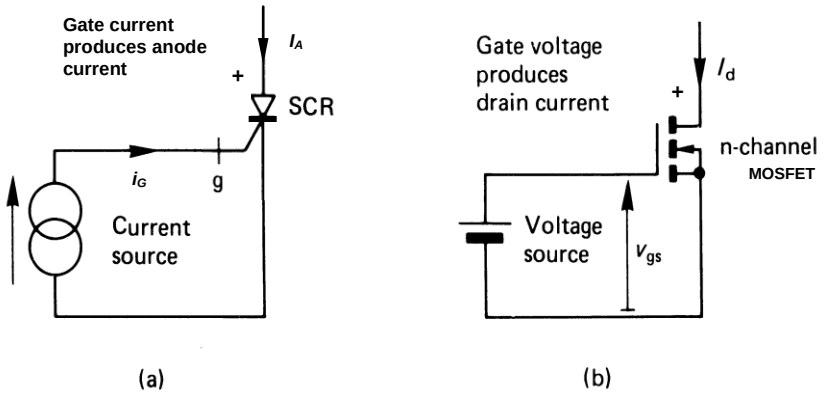


Figure 8.1. *Thyristor and transistor drive requirements: (a) current drive for the bipolar junction thyristor and (b) voltage drive for the MOSFET and IGBT.*

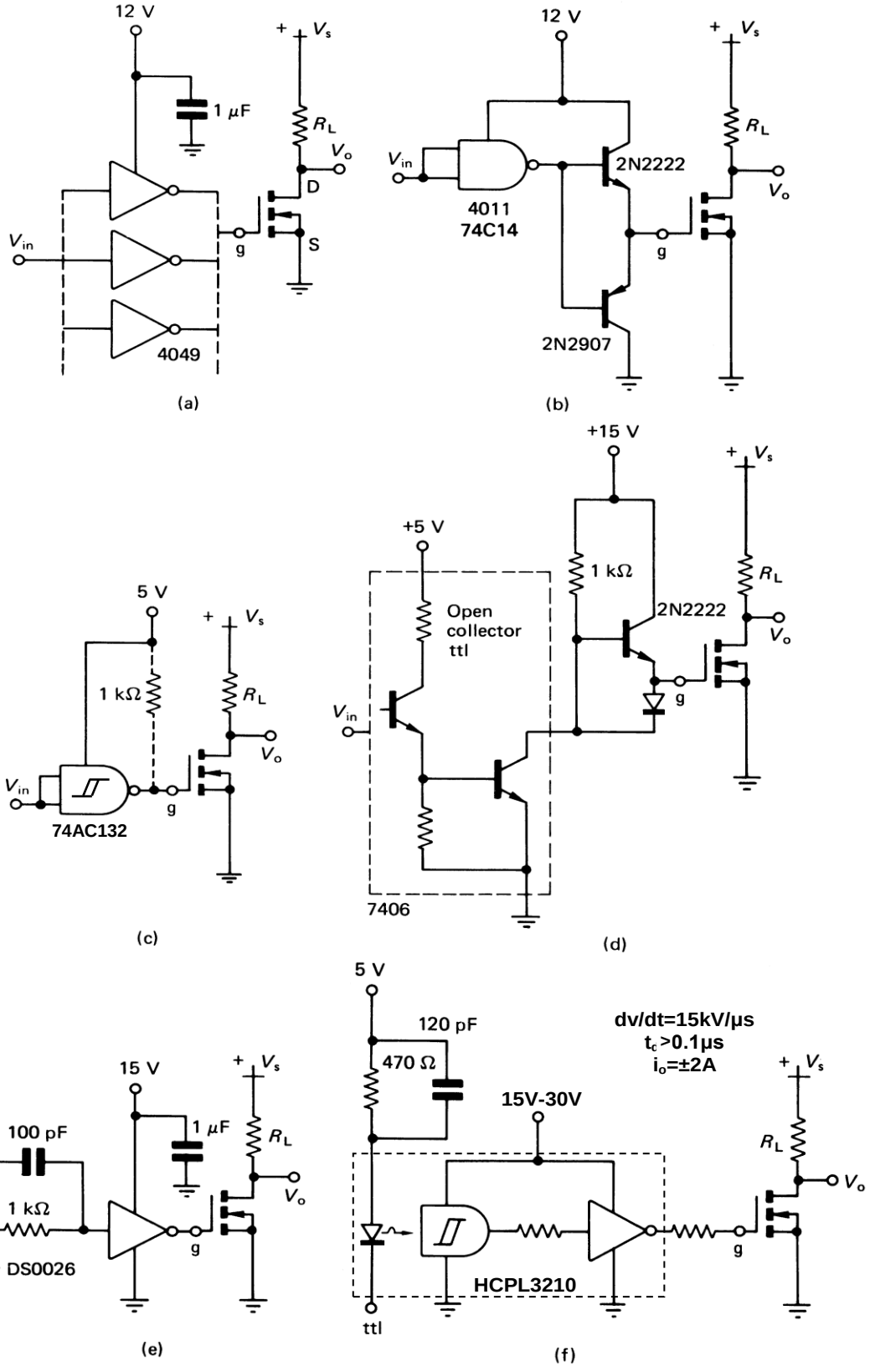
8.1 Application of the power MOSFET and IGBT

The MOSFET gate is isolated electrically from the source by a dielectric layer of silicon dioxide. Theoretically no current flows into the gate when a dc voltage is applied to it. In practice, gate current is required to charge device capacitances and a small leakage current of the order of nano-amps does flow in order to maintain the gate voltage.

When no voltage is applied between the gate and source terminals (but with zero impedance), the drain-to-source impedance is very high and only a small leakage current of less than a milli-amp flows in the drain, until the applied voltage exceeds the drain-to-source avalanche voltage, V_{DSS}.

When a positive gate voltage is applied, an electric field is produced which modulates the drain-to-source resistance. When a gate voltage exceeds the threshold voltage level the channel resistance reduces to a low resistance and drain current flows. The maximum drain current depends on the gate voltage magnitude, assuming that the impedance of the external drain circuit is not current-limiting.

Turn off - reducing the drain current to the leakage current level - is achieved by reducing the gate voltage to below the gate threshold voltage level. The drain switching speeds are essentially determined by that speed at which the gate voltage can reach a level above the threshold voltage (for turn-on) or below the threshold voltage (for turn-off). Although the gate-to-source capacitance is an important parameter, the gate-to-drain capacitance is more significant because of the Miller effect, as considered in section 4.4.2. During switching, the dynamic gate-to-drain capacitance can be effectively much larger than the gate-to-source capacitance. The Miller capacitance typically requires more charge for switching than the gate-to-source capacitance.



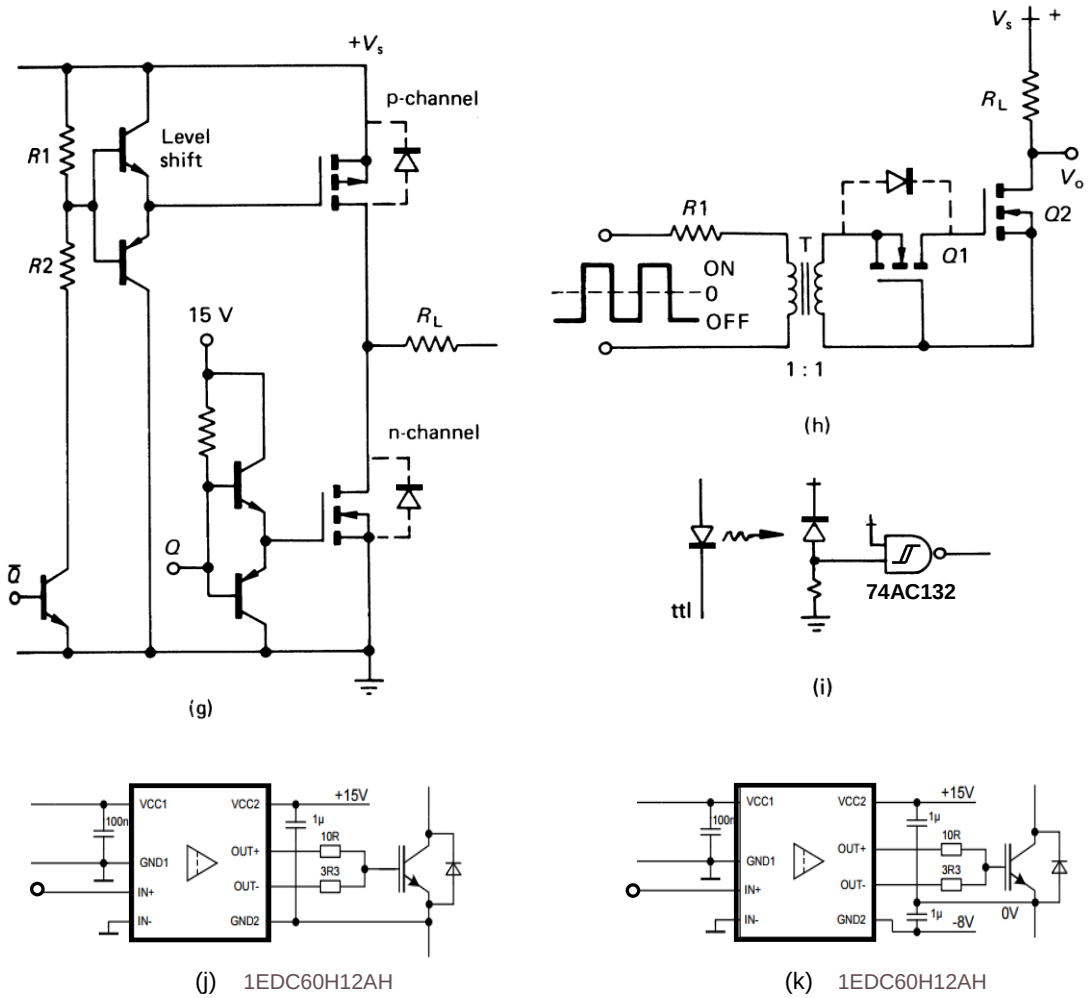


Figure 8.2. *Gate drive circuits for the MOSFET and IGBT: (a) driven from cmos; (b) driven from cmos and an emitter follower; (c) driven from ttl with pull-up resistor which increases sourcing capability; (d) driven from open collector ttl with an external current source; (e) driven from a high-current cmos clock driver; (f) opto-isolated driver circuit; (g) drive circuits for a totem pole connected p and n-channel MOSFET leg; (h) driven from a pulse transformer; (i) fibre optic translation stage, (j) coreless transformer isolation unipolar gate voltage, and (k) coreless transformer isolation bipolar gate voltage.*

8.1.1 Gate drive circuits

The trench gate n-channel enhancement-mode power MOSFET (or IGBT) with a low threshold voltage interfaces easily with logic level integrated circuits. This allows low-power digital logic circuits to control directly high-power levels. Figure 8.2 shows a series of ttl and cmos circuits driving power MOSFETs, each circuit offering different levels of switching speed and performance.

When driving a MOSFET directly from a cmos gate output, as shown in figure 8.2a, only modest rise and fall times can be expected because of the limited source and sink current available from a cmos gate. Figure 8.3a illustrates the output configuration of a typical cmos output stage, which consists of a series-connected p and n-channel MOSFET with the gates connected together. The cmos totem pole output stage is driven by a common signal, hence the name complementary mos - cmos - and when the input is high the n-channel device is on and the p-channel off, while when the input is low, the p-channel turns on and the n-channel turns off. However, cmos has a limited current output capability as shown in the 4049 source-to-sink output characteristics in figure 8.3b and c. The cmos gate output has to drive as a load the power MOSFET capacitive gate. In this configuration, the turn-on current is supplied from the p-channel fet, which has the poorer characteristics of the cmos pair. The turn-off current is sunk by the n-channel fet. Table 8.1 shows cmos typical current source and sink capabilities, switching speeds, and output impedance. It will be seen that the best performance, by far, is achieved from the 4049 and 4050 buffers.

If shorter delays and faster drain rise and fall times are required there are several ways to obtain them. The simplest is to parallel a number of identical cmos inputs and outputs as shown dotted in figure 8.2a. The additional current capability, with the six parallel connected gates of the 4049, will significantly improve MOSFET switching performance.

In figure 8.2b the gate drive current is the output current of the cmos gate multiplied by the gain β of the bipolar transistors. No bipolar saturation times are incurred since the transistors are operating as emitter followers, which cannot saturate. The operating frequency is no longer restricted by the cmos output current limitations.

MOSFETs can also be driven directly from ttl gates. Table 8.2 shows ttl typical current source and sink capabilities and switching speeds. Low supply voltage, typically 5V, and high internal sourcing impedance characteristics, restrict MOSFET switch-on speed and gate voltage level. The ttl sink capability is significantly higher than source capability, hence a pull-up resistor as shown in figure 8.2c enables the sinking capability to be exploited at turn-on, as well as at turn off. A limitation of using ttl for driving MOSFETs is that the gate voltage is restricted to less than 5V, hence if the drain current is not to be restricted, low gate threshold voltage trench gate MOSFETs and IGBTs are used. An open collector ttl drive technique as shown in figure 8.2d overcomes the gate voltage limitation as well as improving the current source limit.

Very fast switching speeds are attained with the capacitive driver shown in figure 8.2e. Such drivers can both source and sink typically 1.5 A in tens of nanoseconds. An isolated gate-to-source drive version is shown in figure 8.2f, where a floating 15 V rail is used and the gate control signal is optically transmitted with high *dv/dt* capability. The driver incorporates high current output, with modest propagation delays.

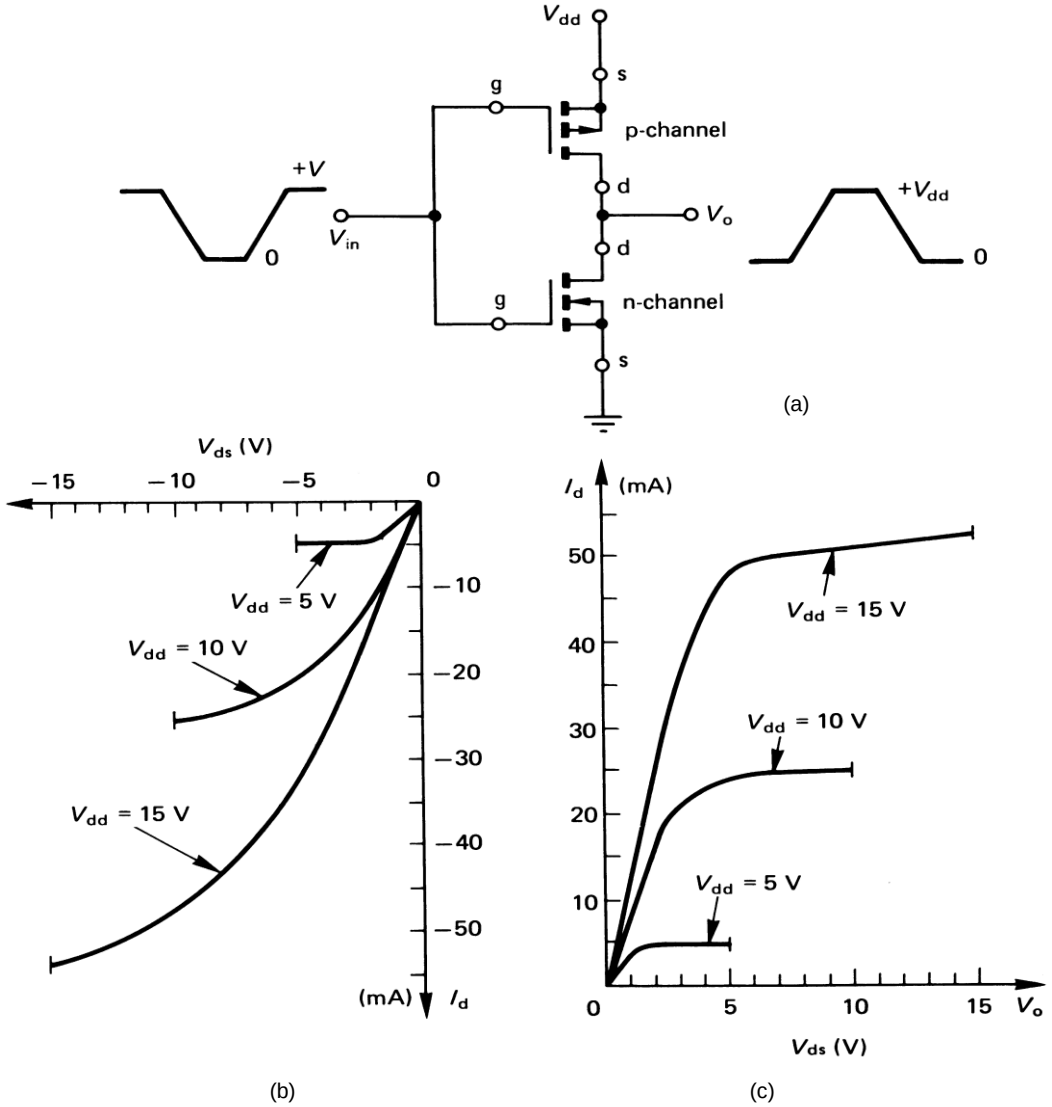


Figure 8.3. *CMOS 4049 inverter output: (a) output cmos totem pole; (b) p-channel drain sourcing; and (c) n-channel drain sinking, both at 25°C.*

Table 7.1 Driving mosfets from cmos (buffered)

Logic conditions			*Standard buffered outputs at logic supply voltage (V_{dd}) of*			*4049/4050 drivers at logic supply voltage (V_{dd}) of*		
			5 V	*10 V*	*15 V*	*5 V*	*10 V*	*15 V*
Logic zero								
Approximate sink current I_{OL} (mA) for $V_{OL} \leqslant 1.5$ V			1.5	3.5	4.0	20	40	40
Logic one								
Minimum source current I_{OH} (mA) for V_{OH}			−0.51 ⩾4.6 V	−1.3 ⩾9.5 V	−3.4 ⩾13.5 V	−1.25 ⩾2.5 V	−1.25 ⩾9.5 V	−3.75 ⩾13.5 V
Typical switching times (ns) of logic drive signals:								
Rise			100	50	40	100	50	40
Fall			100	50	40	40	20	15
$R_{ds(on)}$ (ohms) (calculated)	Source	Typ.	1.7k	500	430			
		Max.	12.5k	2.5k	–			
	Sink	Typ.	500	420	190			
		Max.	2k	1k	–			

Table 7.2 Driving mosfets from TTL

Logic conditions	*Logic type*								
	74	*74AC*	*74L*	*74LS*	*74S*	*74ALS*	*74HC*	*DS0026*	*Open collector 74, 30 V*
Logic zero									
Min. sink current I_{OL} for V_{OL} = 0.4 V (mA)	16	24	3.6	8	20	18	4	1.5A	40
Logic one									
Max. source current I_{OH} for V_{OH} = 2.4 V (mA)	−0.4	−24	−0.2	−0.4	−1.0	−0.4	−4	−1.5A	22
Typical gate propagation delay (ns)	10	7	50	12	4	4	10	15	12
V_{iL} max. (V)	0.8	1.35	0.7	0.8	0.8	0.8	0.9	—	0.8
V_{iH} min. (V)	2.0	3.15	2.0	2.0	2.0	2.0	3.15	—	2.0

Drive circuits for p-channel MOSFETs may be complicated by the reference signal voltage level, as shown in the series n and p-channel totem pole in figure 8.2g. This figure illustrates how the p-channel drive may be derived by means of a level shifter. The emitter follower, pnp transistor used for turn-on must have a breakdown voltage rating in excess of the totem pole rail voltage. Above 300 V the pnp transistor can be replaced by a diode as shown in figure 8.2d, or a low current high voltage MOSFET. Restricted charging of the translation MOSFET output capacitance can lead to increased delay times. The resistor divider, *R1-R2,* ensures that the p-channel gate voltage limit is not exceeded. In order to increase gate drive capability *R2* can be decreased provided a 15 V Zener is used across the p-channel MOSFET gate to source. The low-voltage npn transistor in the p-channel driver stage is used for fast turn-off, shorting the p-channel source to its gate.
A simple method of driving an n-channel MOSFET, with its source not referenced to ground, is shown in figure 8.2h. Electrical (galvanic) isolation is achieved by means of a pulse transformer. The internal parasitic diode in Q1 provides the path for the n-channel MOSFET gate to charge. When the pulse transformer saturates, Q1 blocks any discharge of the gate until turn-off, when a negative transformer pulse turns on Q1, thereby discharging the n-channel gate charge.
An alternative translation method using a fibre optic stage is shown in figure 8.2i. The temperature-independent, high threshold characteristics of 74AC technology is used for a simple detector comparator.
A Schmitt input (hysteresis) gate (74AC132) improves noise immunity.

In general, translation from ttl levels can be achieved with Zener diode bias circuits.

Table 8.3 show the electrical characteristics of a range of commercial gate drive ICs.

Table 8.3: Gate driver summary

Part Number	Isolated	Isolation Voltage	Operating Supply Voltage	On speed (typical)		Off speed (typical)		Output Peak Sink Current (A_{pk})	Output Peak Source Current (A_{pk})	Input Signal Compatibility	Output Channels	Types
				t_{rise} (ns)	t_{pd} (ns)	t_{fall} (ns)	t_{pd} (ns)					
FAN3278	No	na	8V - 27V	17	45	8	35	1	1.5	TTL	$Q, \bar{Q}$	Low-side
FAN3121/3122	No	na	4.5V - 18V	23	23	19	23	11.4	10.6	TTL/CMOS	1	Low-side
FAN73711	No	na	10V - 20V	25	150	15	150	4	4	TTL	1	High-side (bootstrap)
FAN7190-F085	No	na	10V - 22V	25	140	20	140	4.5	4.5	TTL	2	High and Low-side
IRS21850S	No	na	10V - 20V	15	160	15	160	4	4	CMOS/LSTTL	1	High-side (bootstrap)
IRS2186	No	na	10V - 20V	22	170	18	170	4	4	TTL	2	High and low-side
EL7158	No	na	4.5V - 12V	12	22	12.2	22.5	12	12	TTL	1	Low-side
ISL6700	No	na	9V - 15V	5	45	5	75	1.3	1.4	TTL	2	High and Low-side
IXDD430	No	na	8.5V - 35V	18	41	16	35	30	30	TTL/CMOS	1	Low-side
ACPL333J	Yes	3.75kV	15V - 30V	50	180	50	180	2.5	2.5	Input current limit: 12mA	1	Opto-coupler
ACNW3190	Yes	5kV	15V - 30V	100	300	100	300	5	5	Input current Limit: 25mA	1	Opto-coupler
PC925L0NSZ0F	Yes	5kV	15V - 30V	100	300	100	300	2.5	2.5	Input current Limit: 25mA	1	Opto-coupler
1EDI60H12AH	Yes	1.2kV	3.1V-17V	20	120	19	125	6	6	3V-15V	1	Coreless transformer
1EDC60H12AH	Yes	1.2kV	13V-35V	10	300	9	300	10	9.4	<17V	1	Coreless transformer

From the circuits in figure 8.2 it is seen that there are two basic types of gate drives.

- Low-side
- High-side

Essentially a low-side driver is one where the control signal and the power device gate are at almost the same potential. The lower switches in bridge legs normally use low-side drivers, while the upper switches require high-side drivers which translate the control signal and gate power to a different

potential. The gate drive circuits 8.2a to 8.2e are basic low-side gate drive circuits. The high-side drivers in figures 8.2f to 8.2k translate the control signal to the gate level.

Although the gate drive circuits in figures 8.2a to 8.2k translate the control signal to the device gate, these circuits do not address two important gate drive issues.

- The derivation of the gate drive supply, particularly for floating gate drives as encountered in inverters.
- The derivation of negative gate bias at turn-off for better immunity to false turn-on due to noise and induced Miller charging effects (except the gate drive in figure 8.2j/k).

8.1.1i - *Negative gate drive*

Most of the gate drive circuits shown in figure 8.2 only clamp the gate to near zero volts during the off period. The lower bridge leg switch in figure 8.4 uses ±15V gate voltages. The complementary buffers drive the gate-source of the shown device in an H-bridge configuration. The buffers require an isolated 15V dc supply. Since the 15V dc supply is isolated, the complementary buffers can be used for high side gate drives, provided the control signal is isolated, as in figure 8.2i. Practically a negative gate bias of -5V (as in figure 8.2k) is sufficient for noise immunity while any voltage in excess of this unnecessarily increases turn-on delay and increases gate power requirements. Manufacturers are continually improving power device properties and characteristics. Gate threshold voltage levels are constantly being decreased, and coupled with the fact that the threshold voltage decreases with temperature, negative voltage gate drive is necessary for high noise immunity to prevent false turn-on with high power devices. Gate capacitance improves noise immunity.

8.1.1ii - *Floating power supplies*

There are three basic methods for deriving floating power supplies for gate drives.

- A low inter-winding capacitance, high-frequency transformer
- A capacitive coupled charge pump
- A diode bootstrap

The upper bridge leg switch T_u in figure 8.4 uses both a diode bootstrap via D_{bs} and a single ended capacitor charge pump via C_{cp}, in order to derive gate power.

1 *- capacitive coupled charge pump*

By switching T_{cp} at high frequency the low-capacitance, high-voltage capacitor C_{cp} is successively charged through D_{cp1} and discharged through D_{cp}. Discharge through D_{cp} involves charging C_{gs}, the gate voltage supply capacitor. The shown charge and discharge paths both rely on either the upper switch T_u or diode D_u being in a conducting state.

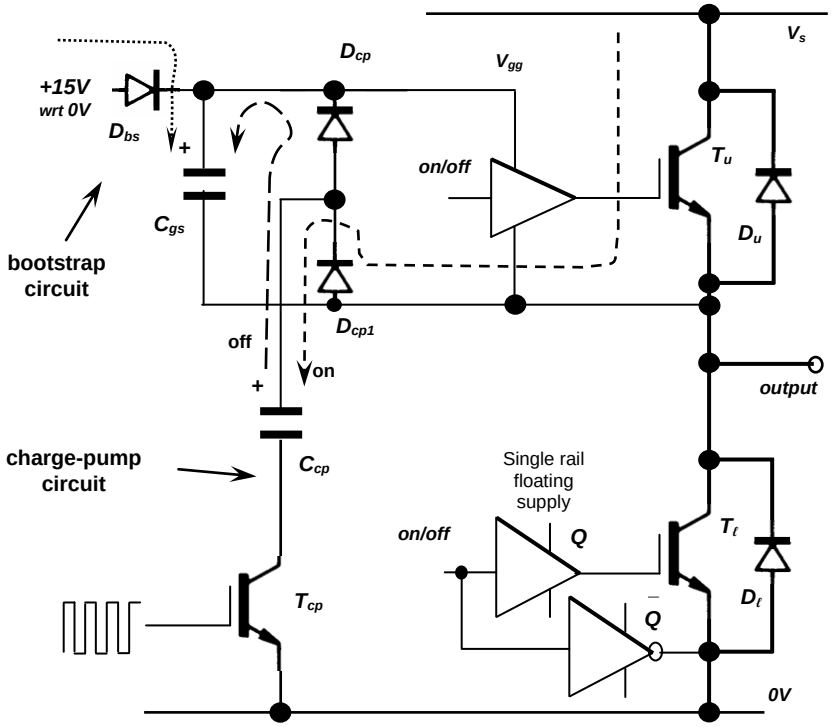


Figure 8.4. *Typical IGBT bridge leg showing ±15V gate drive on the leg lower switch and charge pump plus boot strap gate supply circuits for the leg upper switch.*

2 *- diode bootstrap*
When the lower switch T_ℓ or diode D_ℓ conduct, high voltage diode D_{bs} allows the upper gate supply capacitor C_{gs} to charge from a 15V dc supply which is referenced to the 0V dc rail. When the upper switch or diode conduct, the bootstrap diode is reverse bias and supports $V_s + V_{gg}$. Start-up is a problem since the gate of the upper switch T_u is in a high impedance state while its supply is being charged after the lower switch is turned on. For this reason, the bootstrap is usually used in conjunction with a capacitor charge pump.

The only foolproof method to ensure gate power at all times, particularly at start-up and during prolong on-state periods, is to use a high-frequency (power and/or signal) transformer approach. DC to dc converters of a few Watts offer isolation up to 5kV to 10kV.

Figure 8.5 shows the implementation of gate voltage supplies derived via a current sourcing technique. The single conductor co-axial primary is common to all *N* gate levels, and is located concentrically to provide the necessary electrical isolation, creepage, and clearance, for high voltages series connection of devices.
The single conductor is fed from a square wave ac controlled source current (current from an output inductor in a full bridge converter with source voltage V_{DC}). The secondary (of *n* turns) of one or more windings at each level are rectified. The lowest rectified secondary voltage (seen as a short circuit secondary by the primary) is charged until all the secondary voltages are equal. Because the primary has a controlled current, any quasi short circuit rectified secondary is controlled and obeys Ampere's law, $N_pI_p=nI_s$, where N_p=1. The primary current being a controlled current means every level can be charged from zero volts. That is, when any secondary rectified voltage is less than the open circuit voltage, it is current source charged. Current transfer ceases when the sum of the reflected rectified secondary voltages match the voltage source driving the current source inductor. That is, when

$$V_{DC} = \sum_{i=1}^{N} V_{si} \Big/ n_{si}$$

Figure 8.5. *Gate level isolated power supplies for series connected devices.*

8.1.2 Gate drive design procedure

The effective gate to source capacitance, C_{in}, can be calculated from

$$C_{in} \triangleq \delta Q_g \,/\, \delta V_{gs} \qquad (8.1)$$

The initial slope of the charge in figure 8.6a, 740 pF, is due to the gate source capacitance charging below the gate threshold level. The next charge section between Q_{g1} and Q_{g2} in figure 8.6c is due to the Miller effect. The horizontal charge portion is due to the very high drain-source depletion field capacitance as the drain falls below the gate voltage level.
The drain switching times, similar to those derived in 4.4.2, can be calculated from the charge transfer characteristics in figure 8.6, using the following equations.

(i) From figure 8.6c, for turn-on

$$t_{d\ on} = \frac{Q_{g1}}{V_{g1}} R_g \ \ell n \left(\frac{V_{gg}}{V_{gg} - V_{g1}}\right) \quad \text{(s)} \tag{8.2}$$

$$t_r = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_g \ \ell n \left(\frac{V_{gg} - V_{g1}}{V_{gg} - V_{g2}}\right) \quad \text{(s)} \tag{8.3}$$

(ii) From figure 8.6d, for turn-off

$$t_{d\ off} = \frac{Q_{g2} - Q_{g2}}{V_{g2} - V_{g2}} R_g \ \ell n \ \frac{V_{gg}}{V_{g2}} \quad \text{(s)} \tag{8.4}$$

$$t_f = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_g \ \ell n \ \frac{V_{g2}}{V_{g1}} \quad \text{(s)} \tag{8.5}$$

where R_g is the gate equivalent series resistance and $V_{g1} = V_{TH}$.

The energy required for switching is given by

$$W = \tfrac{1}{2} Q_{g3} V_{gg} \quad \text{(J)} \tag{8.6}$$

which is dependent on the drain current and voltage. The gate drive power requirements are given by

$$P = Q_{gs} \ V_{g3} \ f_s \quad \text{(W)} \tag{8.7}$$

Obviously the faster the switching speed requirement, the higher and faster the gate drive current delivery necessary.

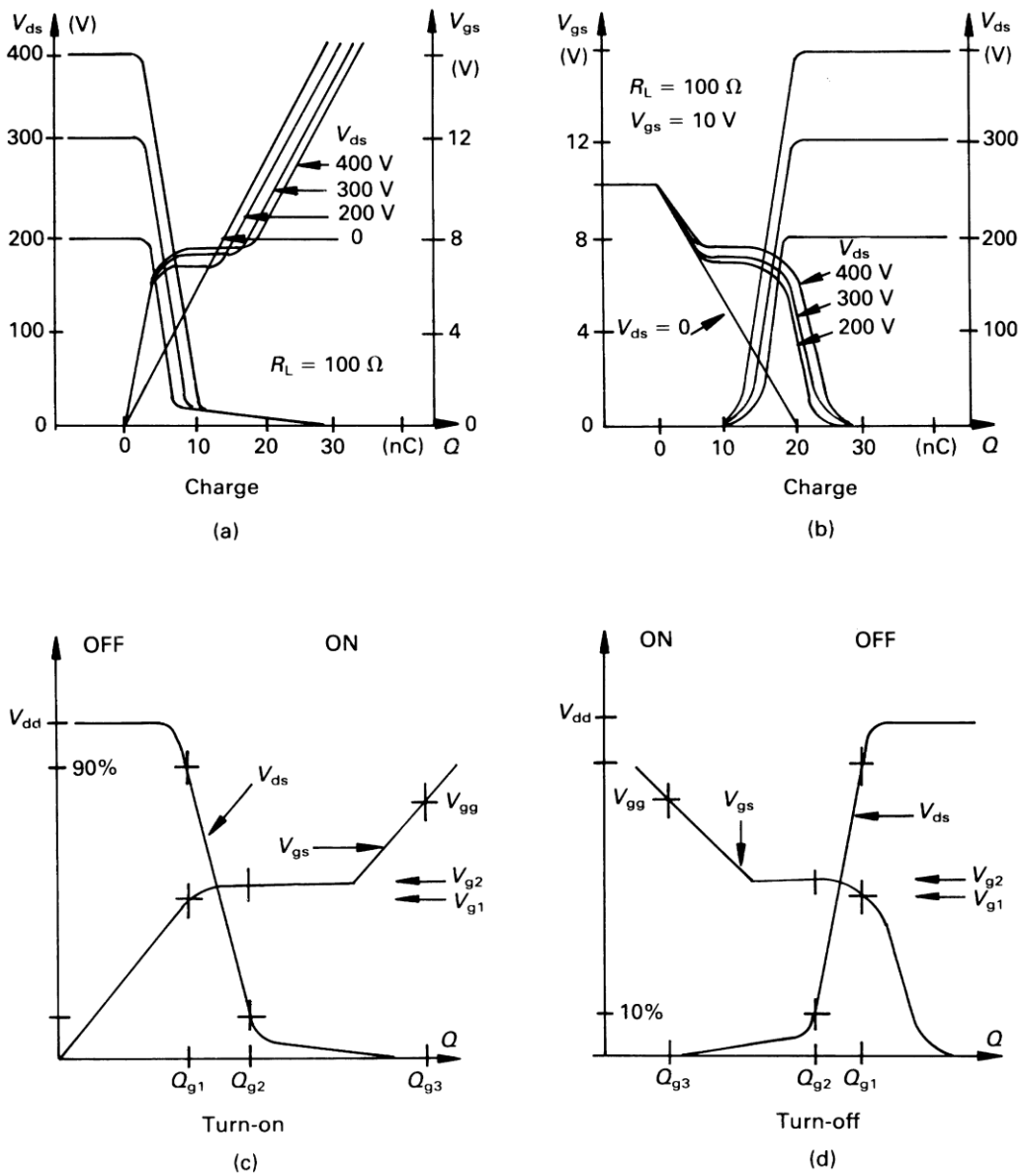


Figure 8.6. *Typical MOSFET charge transfer characteristics at: (a) turn-on; (b) turn-off; (c) turn-on showing switching parameters; and (d) turn-off showing switching parameters.*

If only 15 mA is available for gate drive then, based on figure 8.6, switching occurs in about 1 µs (from $Q = I \times t$). This level of performance could be expected with circuit 8.2a, and slower switching for the circuit in figure 8.2c. By employing the gate drive in figure 8.2c, the gate voltage is limited to 5 V, hence the MOSFET represented by figure 8.6 could not be switched.
The circuits in figures 8.2b and 8.2d are capable of delivering about 100 mA, which yields switching speeds of the order of 150 ns, with only 50 mW of drive power dissipation at 100 kHz. The drive circuit in figure 8.2e is capable of delivering ±1.5 A. Hence the device characterised by figure 8.6 can be switched in only 10 ns.

Switching times deteriorate slightly if reverse gate-to-source biasing is used for higher noise immunity in the off-state. Analysis of the increase in turn-on delay as a result of the use of negative gate drive is presented in Appendix 4.8.

Example 8.1: ***MOSFET input capacitance and switching times***

A MOSFET switching a resistive load has the following circuit parameters:

$$R_g = 47\Omega, \qquad R_L = 100\Omega$$
$$V_{gg} = 10\text{ V}, \qquad V_{ds} = 400\text{ V}$$

Based on the charge transfer characteristics in figure 8.6, calculate the gate input capacitance and switching times for MOSFET turn-on and turn-off.

Solution

The charge transfer characteristics shown in figure 8.6 are valid for a 100 Ω resistive load and a 0-10 V gate voltage. A 400 V drain switching characteristic is shown.

At turn-on, from figure 8.6a and using equations (8.2) and (8.3)

(i) $C_{in} = C_{gs} = Q_{g1} / V_{g1} = 4.4\text{ nC} / 6\text{V} = 740\text{ pF}$
$t_{d\,on} = 740\text{ pF} \times 47\Omega\ \ell n\ (10\text{V}/10\text{V}-6\text{V}) = 31.9\text{ ns}$

(ii) $C_{in} = (Q_{g2} - Q_{g1}) / (V_{g2} - V_{g1}) = 5.6\text{ nC} / 1.5\text{V} = 3.7\text{ nF}$
$t_r = 3.7\text{ nF} \times 47\Omega\ \ell n\ 5.6\text{V}/2.5\text{V} = 141.3\text{ ns}$

At turn-off, from figure 8.6b and using equations (8.4) and (8.5)

(i) $C_{in} = (Q_{g3} - Q_{g2}) / (V_{gg} - V_{g2}) = 7.5\text{ nC} / 2.5\text{V} = 3\text{ nF}$
$t_{d\,off} = 3\text{ nF} \times 47\Omega\ \ell n\ 10\text{V}/7.5\text{V} = 40\text{ ns}$

(ii) $C_{in} = (Q_{g2} - Q_{g1}) / (V_{g2} - V_{g1}) = 7.5\text{ nC} / 0.9\text{V} = 8.3\text{ nF}$
$t_f = 8.33\text{ nF} \times 47\Omega\ \ell n\ 7.5\text{V}/6.6\text{V} = 50\text{ ns}$

An underestimate of the fall time results if figure 8.6a is used for both turn-on and turn-off calculations ($C_{in} = 3.7$ nF and $t_f = 39.1$ ns).

♣

8.2 Application of the thyristor

The basic gate requirements to trigger a thyristor into the conduction state are that the current supplied to the gate is

- of adequate amplitude and sufficiently short rise time
- of sufficient duration.

The gate conditions are subject to the anode being forward-biased with respect to the cathode. Figure 8.7 illustrates a typical thyristor gate current waveform for turn-on.
The initial high and rapid current quickly turns on the device so as to increase the anode initial *di/dt* capability. After a few microseconds the gate current can be decreased to a value in excess of the minimum gate requirement. After the thyristor has latched on, the gate drive may be removed in order to reduce gate power consumption, namely the losses. In some inductive load applications, where the load current lags, a continuous train of gate pulses is usually applied to ensure turn-on.
Gate drives can be divided broadly into two types, either electrically isolated or non-isolated. To obtain electrical isolation usually involves the use of a pulse-transformer or an opto-coupler but above a few kilovolts fibre-optic techniques are applicable.

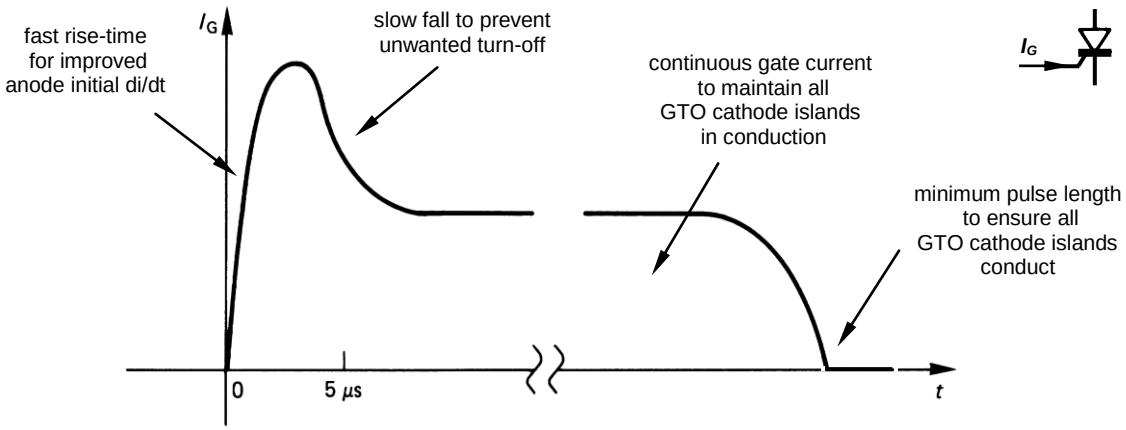


Figure 8.7. *Ideal thyristor gate current waveform for turn-on.*

8.2.1 Thyristor gate drive circuits

Only low-power thyristors with amplifying gates can be triggered directly from ttl or cmos. Usually a power interface stage is employed to convert ttl current sink and source levels of a few milliamps up to the required gate power levels.

Figure 8.8a and b shows two power interface circuits for triggering a triac. The triac could equally be another thyristor device. An important safety default feature of both these circuits is that no active device exists between the gate and Ml. During the off-state the gate is passively clamped by the resistor R_g to a voltage well below the minimum voltage level for turn-on.

Bidirectional gate current can bring the triac into conduction. Figures 8.8c and d show how negative gate turn-on current can be derived.

If electrical isolation between the control circuitry and the power thyristor circuit is required, a simple triac opto-coupler can be employed as shown in figure 8.8e. The photo-triac is optically turned on which allows bidirectional main triac gate current to flow, the magnitude of which is controlled by the high-voltage resistor R_g. If the main device is an SCR, an opto-coupled SCR can be used for isolation and uni-direction gate triggering current.

When suitable voltage rails are not available or isolation is required, a pulse transformer drive circuit can be employed as shown in figure 8.8f. The diode/Zener diode series combination across the pulse transformer primary provides a path for primary magnetising current decay at turn-off and prevents saturation. The resistor R limits the secondary current into the SCR gate. This resistor can be placed in the pulse transformer primary or secondary by transforming the resistance in the turns ratio squared. If R is in the primary circuit and transformer saturation inadvertently occurs, the resistor R limits the current and protects the switching transistor T_s. The transformer secondary resistor R_2 is employed to decrease the gate to cathode impedance, thereby improving *dv/dt* capability, while the gate diode D_r prevents possible reverse gate voltage breakdown after T_s is turned off and the output voltage reverses during core reset. For core reset, the transformer duty cycle must satisfy $t_{off} V_z \geq t_{on} V_s$, neglecting R.

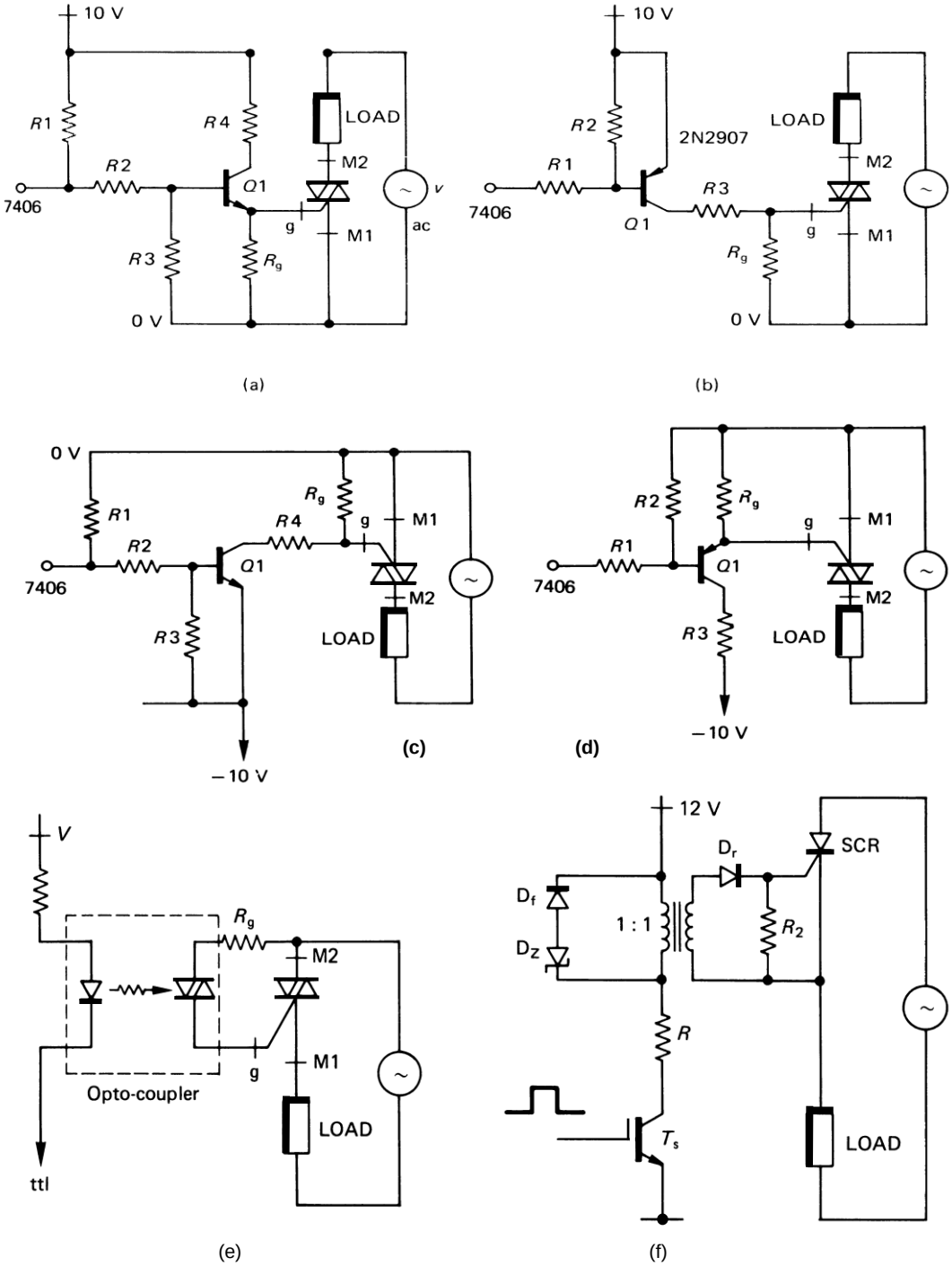


Figure 8.8. *Integrated circuit compatible triac gate drive circuits: (a) high level ttl activation; (b) low level ttl activation using an interfacing pnp transistor; (c) negative gate drive interface with high ttl output for triac activation; (d) negative gate drive interface with low ttl level for triac turn-on; (e) a triac opto-coupler isolated gate drive used to gate-drive a higher power triac; and (f) a pulse transformer drive isolated gate drive for a thyristor.*

i. Vacuum cleaner suction control circuit

In the vacuum cleaner suction control circuit in figure 8.9a the triac is the power control element, itself controlled by a diac which is switched on by charging of C_1 through potentiometer R_2. The resistance of the diac is virtually infinite as long as its voltage it remains within the breakover voltage limits, $\pm V_{BO}$.

During each half cycle of the mains sinewave, C_1 charges until the voltage across it exceeds the diac breakover voltage. The diac then switches on and C_1 discharges into the gate of the triac which then switches on. Diodes D_1 and D_2 stabilise the supply voltage to the charging circuit so that its operation is independent of mains voltage fluctuations.

If $-V_{BO}$ and $+V_{BO}$ are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half sinusoidal cycle. The conduction angle, and therefore the speed of the motor and the cleaner suction, is determined by the adjustment of R_2. Preset potentiometer R_3 sets the minimum suction level. The width and amplitude of the trigger pulses are kept constant by gate resistor R_4. The zinc oxide voltage dependent resistor, U, minimises the possibility of damage to the triac due to high voltage transients that may be superimposed on the mains supply voltage.

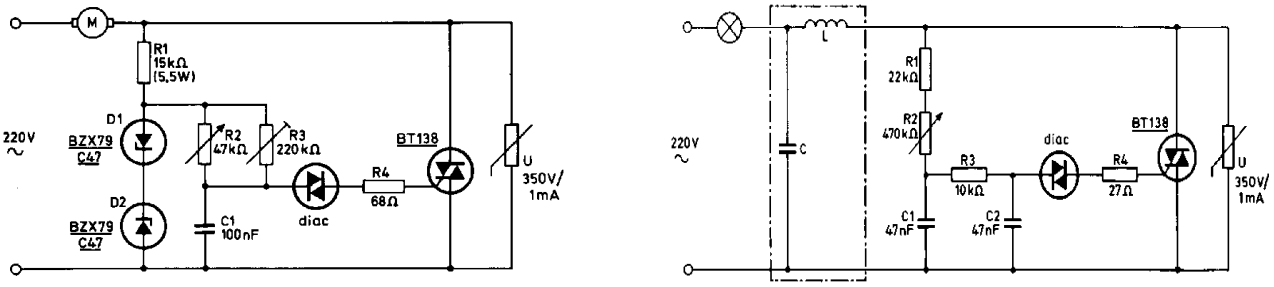


Figure 8.9. *Circuit diagram of: (a) vacuum cleaner suction controller and (b) a lamp dimmer.*

ii. Lamp dimmer circuit

A light dimmer circuit using a triac power control element, triggered via the diac, is shown in figure 8.9b. The potentiometer R_2 determines the phase difference between the ac mains sine wave and the voltage across C_2. This in turn sets the triac triggering angle, whence the lamp intensity.

The resistance of the diac is high as long as the voltage across it remains within its breakover voltage limits, $\pm V_{BO}$. Each half cycle of the mains charges C_2 via R_1, R_2 and R_3 until the voltage being applied to the diac reaches either of its breakover levels. The diac then conducts and C_2 discharges into the gate of the triac, switching it on. If $-V_{BO}$ and $+V_{BO}$ are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half sinusoidal cycle. C_1 prevents the voltage across C_2 from changing abruptly after triggering, thus preventing progressively alteration of the phase relationship between the mains voltage and voltage across C_2. It thus prevents an undesirable hysteresis effect. The voltage across C_1 partially restores the voltage across C_2 after triggering and thereby minimizes the hysteresis effect. Gate resistor R_4 keeps the width and amplitude of the trigger pulses constant. The VDR minimizes the possibility of the triac being damaged by high voltage transients that may be superimposed on the mains supply voltage.

Some form of filter is needed to comply with regulations concerning conducted and radiated interference. The simple *LC* filter shown within the dashed-lined box in figure 8.9b may be adequate. The values of the filter components will vary, but a combination of 0.15mF capacitor and a low *Q* inductor of 2.5mH is generally sufficient for the circuit to meet EMC limits. Circuits with intermittent loads, as with drills, sawing machines, and food mixers, are generally outwith EMC filtering regulations.

iii. Back EMF feedback circuits

A motor speed control circuit, for electric drills, that employs back EMF to compensate for changes in motor load and mains voltage is shown in figure 8.10a. The series resistors R_1, R_2, R_3 and diode D_1 provide a positive going reference potential to the thyristor gate via diode D_2. Diode D_1 is used to reduce the dissipation in the series resistors and diode D_2 isolates the trigger circuit with the thyristor in the on-state. When the thyristor is not conducting the motor produces a back EMF voltage across the armature proportional to residual flux and motor speed. This appears as a positive potential at the thyristor cathode.

A thyristor fires when its gate potential is greater than cathode potential by a fixed amount. Depending on the waveform shape and amplitude at the gate, the circuit may function in several modes.

If, for example, during positive half cycles a constant dc potential was applied at the gate, figure 8.11, the thyristor would continue to fire at the beginning of each cycle until the back EMF was large enough to prevent firing. Thyristor firing would then continue intermittently at the beginning of the positive cycles to maintain some average motor speed.

Referring to figure 8.10a the waveform appearing at the thyristor gate will approximate to a half sine wave, figure 8.10b. As a result, the firing angle must be less than 90° - the most positive value of the trigger potential. At lower motor speeds the firing angle may need to be 130° for smooth operation. If the maximum firing angle is limited to 90° then intermittent firing and roughness motor operation results.

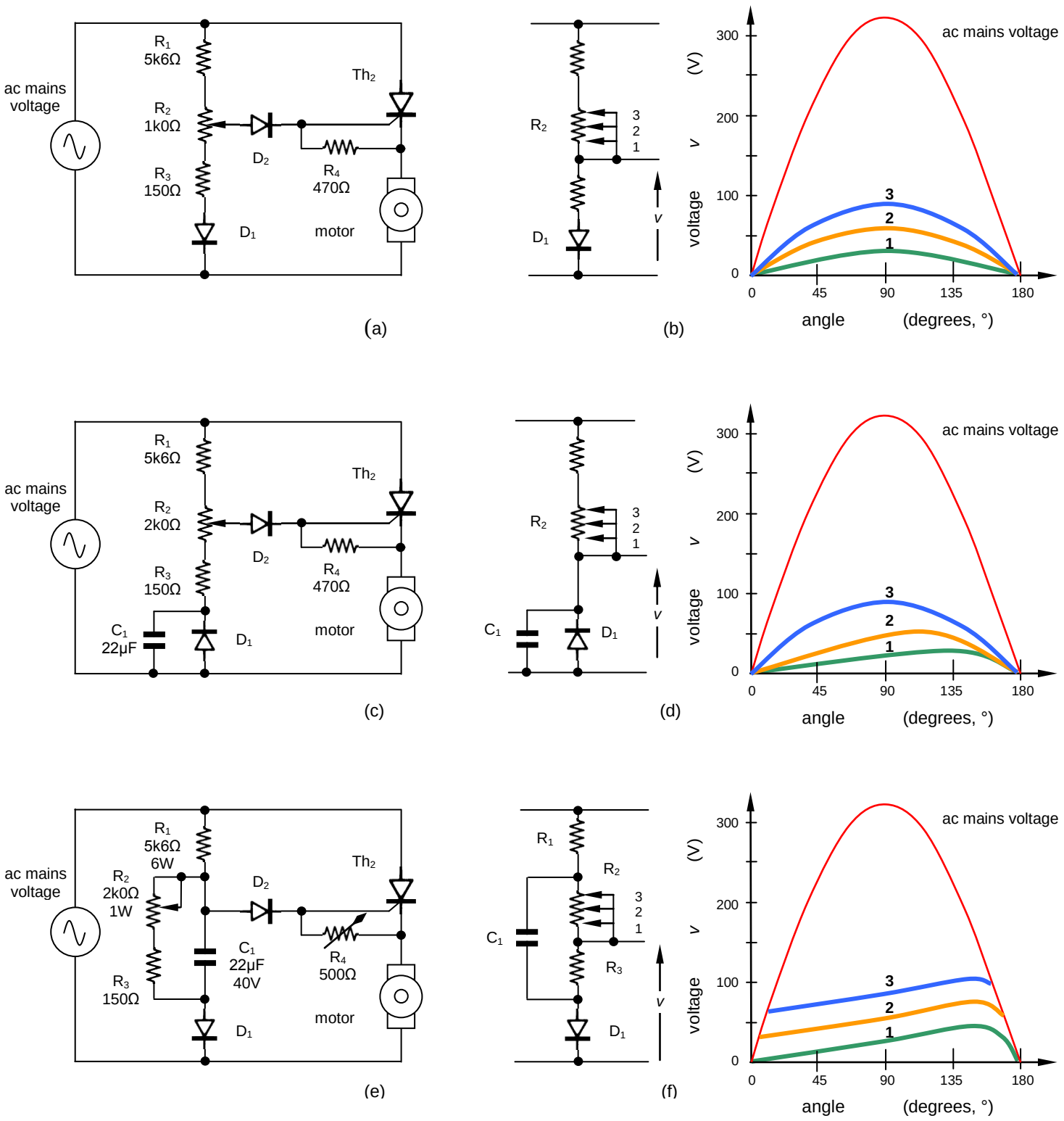


Figure 8.10. *Thyristor speed control circuit and gate waveforms using back EMF feedback: (a) basic controller, (b) improved low speed controller, and (c) improved low and high speed controller.*

If, however, the waveform at the gate has a positive slope value to an angle of at least 130° then it will be possible to have a stable firing point at low speeds. Such a waveform can be produced if there is some phase shift in the trigger network.

Stable Firing at Small Conduction Angles

The trigger network of the circuit shown in figure 8.10c has been modified by the addition of a capacitor C_1 and diode D_1. The diode clamps the capacitor potential at zero during the negative going half cycles of the mains input. The waveform developed across the capacitor has a positive slope to 140°, allowing thyristor triggering to be delayed to this point.

As R_2 is decreased, the peak of the waveform at the gate moves towards 90° as shown in figure 8.10d. As the speed increases, the no load firing angle also advances by a similar amount so stability will be maintained. This circuit will give smoother and more stable performance than the circuit of figure 8.10a. It will, however, give a marginally greater speed drop for a given motor loading at low speed settings. At the maximum speed settings the circuit of figure 8.10a approximates to that of figure 8.10c.

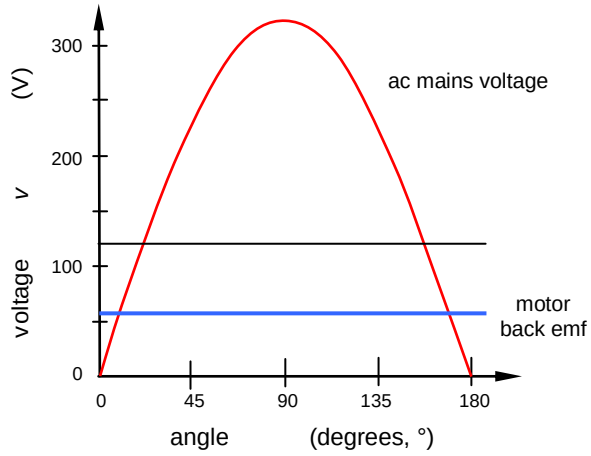


Figure 8.11. *Waveforms with a dc gate supply.*

Improved Motor Performance with Stable Firing

The circuits in figure 8.10 a and c have gate voltage waveforms that are of near linear slope from the zero point of each positive half cycle, as seen in figures 8.10 b and d. This means that the only time that thyristor firing can be advanced in the mains cycle, say at 20°, is when the back EMF and hence motor speed is low. This effect tends to prevent smooth running at high speeds and high loads.

Stable triggering, at low angles, can be achieved if the gate voltage ramp starts each cycle at a small positive level. This means that the time to reach the minimum trigger voltage is reduced. This is achieved by the circuit in figure 8.10e, where the capacitor C_1 is charged during positive half cycles via resistor R_1 and diode D_1. During negative half cycles the only discharge path for capacitor C_1 is via resistors R_2 and R_3.

Diode D_1 also prevents C_1 from being discharged as the thyristor switches off by the inductively generated pulse from the motor. As R_2 is increased, capacitor C_1 is discharged less during negative half cycles but its charging waveform remains substantially unchanged. Hence the result of varying R_2 is to shift the dc level of the ramp waveform produced across C_1.
Diode D_2 isolates the triggering circuit when the thyristor is ON. Resistor R_4 adjusts minimum speed, and by effectively bleeding a constant current, in conjunction with the gate current from the triggering circuit, it enables resistor R_2 to give consistent speed settings.

Circuit Design

If the speed controller is to be effective it must have stable thyristor firing angles at all speeds and give the best possible speed regulation with variations of motor load. The circuit in figure 8.10e gives a motor performance that satisfies both these requirements.

There are two factors that are important in the circuit operation in order to obtain the mentioned requirements.

- the value of positive slope of the waveform appearing at the thyristor gate.
- the phase angle at which the positive peak gate voltage is reached during a positive half cycle of ac mains input.

As described, the charging of capacitor C_1 through resistor R_1 determines the rate of rise of voltage at the thyristor gate during the positive half cycle. However, resistor R_1 must also have a resistance such that several times the maximum thyristor gate current passes through the *RC* network to D_1. This current will then give consistent speed settings with the spread of thyristor gate currents when the minimum speed is set by resistor R_4.

The positive slope value of the thyristor gate voltage is fixed according to the motor used. A motor that gives a smooth back EMF voltage will allow a low slope value to be used, giving good torque speed characteristics.

Some motors have coarser back EMF waveforms, with voltage undulations and spikes, and a steeper slope of thyristor gate voltage must be used in order to obtain stable motor operation. Capacitor C_1 is chosen to provide the required positive slope of the thyristor gate voltage.
Analysis of the circuit of figure 8.10e allows the simplified form in figure 8.12a, where it is assumed that current flowing to the thyristor gate is small compared with the current flowing through resistor R_1. An expression can be derived for the voltage that appears at the anode of D_2 in terms of R_1, R_2 and C_1. Specific component values give the thyristor gate waveforms shown in figure 8.12b.

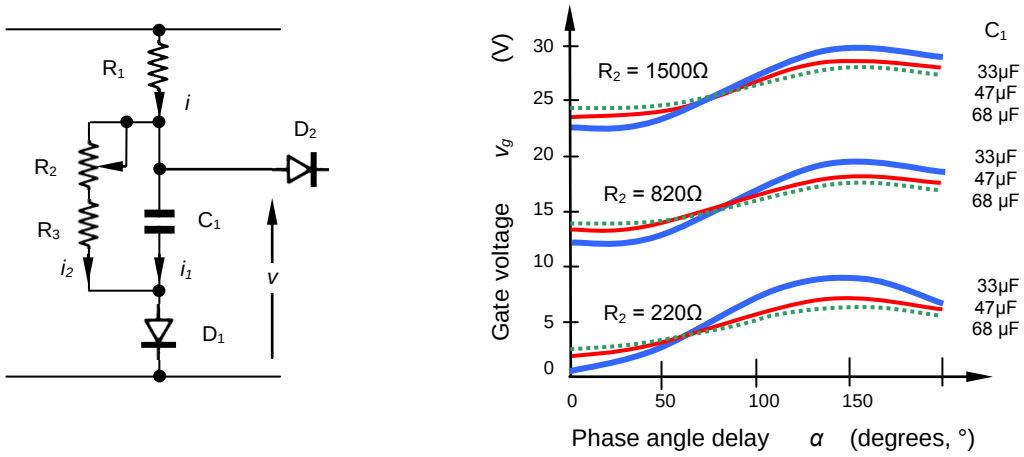


Figure 8.12. *Improved controller: (a) simplified firing circuit and (b) calculated gate waveforms.*

In order to adjust the circuit to match a given motor, the back EMF of the motor must be known. This may be measured using the arrangement shown in figure 8.13. The voltage appearing across the motor is measured during the period when the series diode is not conducting (period A). The voltage so obtained will be the motor back EMF at its top speed on half wave operation, and corresponds to the back EMF that would be obtained from the unloaded motor at its highest speed when thyristor controlled. In practice, since the mains input is a sine wave, there is little increase in the 'no load' speed when the firing angle is reduced to less than about 70°.

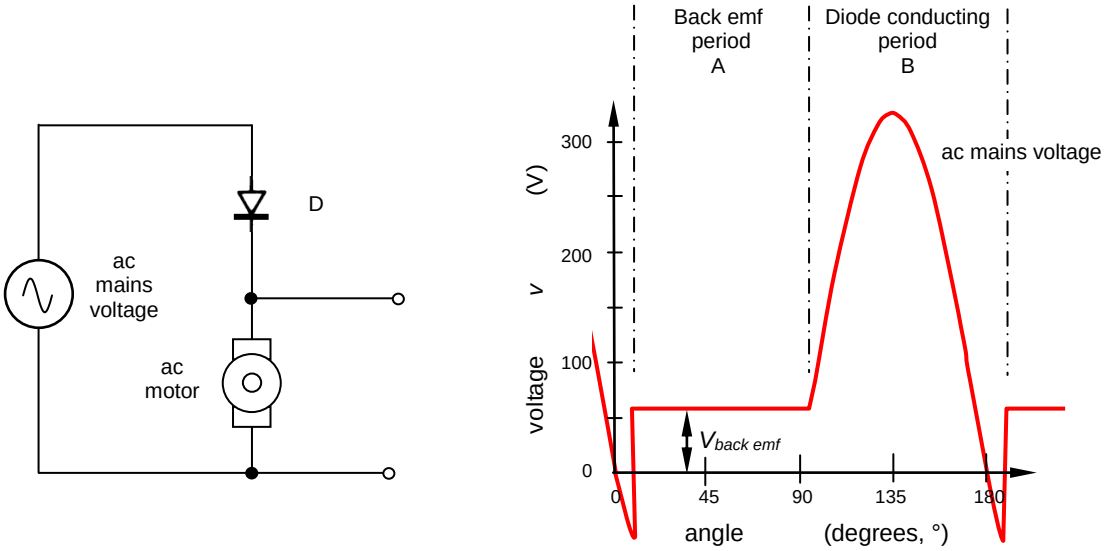


Figure 8.13. *Back EMF measurement circuit and typical voltage waveforms.*

The resistance R_2 in figure 8.10e determines the motor 'no load' speed setting. The waveforms of figure 8.12b may be used as a guide to obtaining the resistance value. It must be chosen so that at 70° and at its highest value, the gate voltage is higher than the measured back EMF by about 2V - the forward gate/cathode voltage of the thyristor.

The thyristor is turned ON when a trigger waveform, shown in figure 8.12b, exceeds the back EMF by the gate/cathode voltage. So, if the back EMF varies within a cycle then there will be a cycle to cycle variation in the firing angle. Normally, random variations of the firing angle by 20° are tolerable.

If, for example, there were variations in the back EMF of 1V, then with a firing angle of 70° and a capacitor of 32μF, the variation of firing angle is about 12°. With capacitor values of 50μF and 64μF the firing angles variations are 19° and 25° respectively. Therefore, 50μF is suitable.

Performance

The torque speed characteristics of the three circuits, when used to drive an electric drill, are compared in figure 8.14a. The circuit of figure 9c has a poorer performance than the two other circuits. That of figure 8.10e may be seen to give a similar performance to the circuit of figure 8.10a at low speeds but, at high speeds and torques, it is better. The circuits of figure 8.10 parts c and e provide low speed operation free from the intermittent firing and noise of the figure 8.10a circuit. Figure 8.14b compares the circuits of figure 8.10a and e when the load is a food mixer motor.

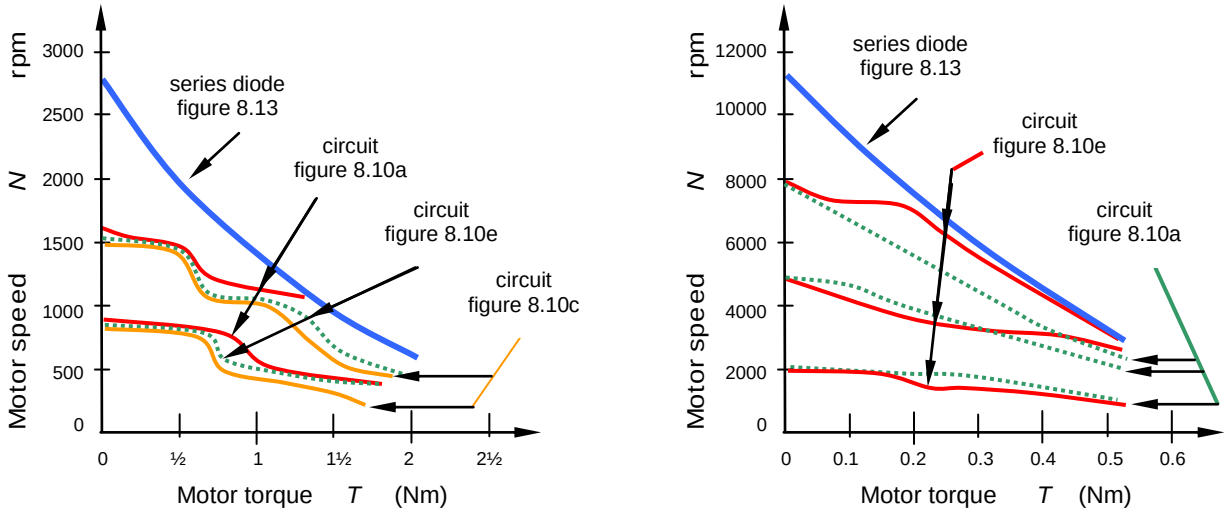


Figure 8.14. *Torque-speed load performance: (a) hand drill and (b) food mixer.*

Circuit Calculations

The following analysis derives an expression for voltage v at the anode of D_2. This expression can be used to produce the gate voltage waveforms shown in figure 8.12b. The analysis assumes that the current drawn by the thyristor gate is negligible in comparison with the current flowing in R_1.

The charging current i_1 for capacitor C_1 in figure 8.12a, is given by:

$$i_1 = \frac{dq}{dt} = C_1 \frac{dv}{dt}$$

and

$$i_1 = \frac{v}{R_2}$$

Representing a mains half sine wave by $f(E)$, where E is the peak mains voltage.

$$i = \frac{f(E) - v}{R_1} = i_1 + i_2$$

Therefore

$$\frac{f(E) - v}{R_1} = C_1 \frac{dv}{dt} + \frac{v}{R_2}$$

where i, i_1 and i_2 are instantaneous currents.

Simplifying

$$C_1 \frac{dv}{dt} + v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{f(E)}{R_1}$$

Fourier analysis of a half sinewave gives:

$$f(E) = E\left\{\frac{1}{\pi} + ½\sin\theta - \frac{2}{\pi}\sum_{n=0,2,4,6..}\frac{\cos n\theta}{n^2 - 1}\right\}$$

Neglecting the Fourier terms for $n > 2$, then

$$C_1 \frac{dv}{dt} + v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{E}{R_1}\left\{\frac{1}{\pi} + ½\sin\omega t - \frac{2}{3\pi}\cos 2\omega t\right\}$$

Then

$$C_1\frac{dv}{dt}+v\left(\frac{1}{R_1}+\frac{1}{R_2}\right)-\frac{E}{\pi R_1}=\frac{E}{R_1}\left\{½\sin\omega t-\frac{2}{3\pi}\cos 2\omega t\right\}$$

Solving for v, the voltage that the trigger circuit would apply to the gate (assuming the gate draws no current), assuming $R_1+R_2 >> \sqrt{2\omega C_1 R_1 R_2}$:

$$v=\frac{R_2E}{\pi(R_1+R_2)}+\frac{R_2E}{2\omega^2C_1^2R_1^2R_2^2}\left\{(R_1+R_2)\sin\omega t-\omega C_1R_1R_2\cos\omega t-\frac{2}{3\pi}\omega C_1R_1R_2\sin 2\omega t-\frac{1}{3\pi}(R_1+R_2)\cos 2\omega t\right\}$$

Solving this equation for different C_1 and R_2 values gives the curves shown in figure 8.12b.

8.2.2 Thyristor gate drive design

In order to design a thyristor gate interface circuit, both the logic and thyristor gate requirements must be specified.

Consider interfacing a typical ttl-compatible microprocessor peripheral which offers the following specification

$$I_{OH} = 0.3\text{mA} \ @ \ V_{OH} = 2.4\text{V}$$
$$I_{OL} = 1.8\text{mA} \ @ \ V_{OL} = 0.4\text{V}$$
$$V_{cc} = 5\text{V}$$

These specifications are inadequate for turning on a power thyristor or an optical interfacing device. If the power thyristor gate, worst case requirements are

$$I_{GT} = 75\text{ mA}, \ V_{GT} = 3\text{ V} \ @ \ -65°\text{C}$$

then a power interfacing circuit is necessary. Figure 8.15 shows an interfacing circuit utilising a p-channel MOSFET with the following characteristics

$$C_{gs} = 400\text{ pf} \qquad V_{TH} = 3.0\text{V}$$
$$R_{ds(on)} = 10\text{ ohms} \qquad I_d = 0.5\text{A}$$

The resistor R_1 limits the MOSFET C_{gs} capacitance-charging current and also specifies the MOSFET turn-on time. If the charging current is to be limited to 1.8 mA when V_{OL} = 0.4 V, then

$$R_1 = (V_{cc} - V_{OL}) / I_{OL} \qquad \text{(ohms)}$$
$$= (5\text{V} - 0.4\text{V}) / 1.8\text{mA} = 2.7\text{ kilohms}$$

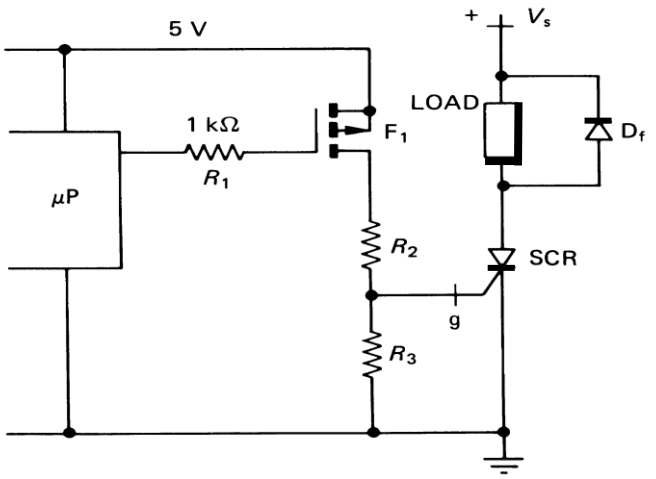


Figure 8.15. *Interfacing a microprocessor to a power thyristor.*

A smaller resistance could be used but this would not preserve the microprocessor low-voltage output level integrity if it were also being used as input to ttl logic. The MOSFET will not turn on until C_{gs} has charged to 3 V or, with a 5 V rail, approximately one R-C time constant. That is

$$t_{delay} = R_iC_{gs} \qquad \text{(s)}$$
$$= 2.7\text{ kilohms} \times 400\text{ pF} = 1\ \mu\text{s}$$

The MOSFET must provide the thyristor gate current and the current through resistor R_3 when the gate is at 3 V.

The maximum value of resistor R_2 is when $R_3 = \infty$ and is given by

$$R_2 = \frac{V_{cc} - V_{GT} - I_{GT} \times R_{ds(on)}}{I_{GT}}$$

$$= \frac{5\text{V} - 3\text{V} - 75\text{ mA} \times 10\Omega}{75\text{ mA}} = 16.6 \text{ ohms}$$

Use $R_2 = 10$ ohms.

The resistor R_3 provides a low cathode-to-cathode impedance in the off-state, thus improving SCR noise immunity. When $V_{GT} = 3$ V

$$I_d = \frac{V_{cc} - V_{GT}}{R_{ds(on)} + R_2} = \frac{5\text{V}-3\text{V}}{10\Omega+10\Omega} = 100 \text{ mA}$$

of which 75 mA must flow into the gate, while 25 mA can flow through R_3. That is

$$R_3 = V_{GT} / (I_d - I_{GT}) \quad \text{(ohms)}$$

$$= 3 \text{ V}/25 \text{ mA} = 120 \text{ ohms}$$

After turn-on the gate voltage will be about 1 V, hence the MOSFET current will be 200mA. Assuming 100 per cent on-state duty cycle, the I^2R power loss in the MOSFET and resistor R_2 will each be 0.4 W. A 1 W power dissipation 10 ohm resistor should be used for R_2.

Example 8.2: ***A light dimmer***

A diac with a breakdown voltage of ±30V is used in a light dimming circuit as shown in figure 8.16. If R is variable from 1kΩ to 22kΩ and C = 47nF, what are the maximum and minimum firing delays? What is the controllable output power range with a 10Ω load resistor?

Solution

The capacitor voltage v_c is given by

$$v_c = \frac{-j/\omega C}{R - j/\omega C} \times 240\angle 0°$$

$$= \frac{1}{1 + j\omega CR} \times 240\angle 0°$$

i. For R = 1 kΩ

$v_c = 237.36 \angle -8.4°$

that is, $v_c = 335.8 \sin(\omega t - 8.4°)$

The diac conducts when v_c = 30V, that is

minimum delay = ωt = 8.4° + $\sin^{-1}$(30V/335.8V) = 13.5°

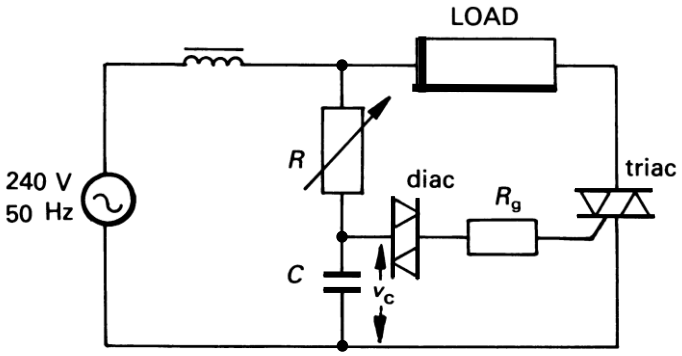


Figure 8.16. *Light dimmer.*

ii. For R = 22 kΩ

$v_c = 70.6 \angle -72.8°$

that is, $v_c = 99.8 \sin(\omega t - 72.8°)$

The diac conducts when v_c = 30V, that is

minimum delay = ωt = 72.8° + $\sin^{-1}$(30V/99.8V) = 92°

The maximum power output, if continuous conduction were possible, is $\hat{P}_o = 240\text{V}^2 / 10\Omega = 5760\text{W}$.

From equation (13.25), the output power for a resistive load is given by

$$P_o = \frac{V_{rms}^2}{R} = \frac{V^2}{R}\left\{1 - \frac{2\alpha - \sin 2\alpha}{2\pi}\right\} \quad \text{(W)}$$

Minimum power at α = 92° (1.6 rad) is $P_o = \frac{240^2}{10\Omega} \times \left\{1 - \frac{2\times 92° - \sin 2\times 92°}{2\pi}\right\} = 2862\text{W}$

Maximum power at α =13½° (0.24 rad) is $P_o = \frac{240^2}{10\Omega} \times \left\{1 - \frac{2\times 13½° - \sin 2\times 13½°}{2\pi}\right\} = 5536\text{W}$

♣

8.3 Drive design for GCT and GTO thyristors

The gate turn-off thyristor is not only turned on from the gate but, as its name implies, is turned off from its gate with negative gate current. Basic GTO thyristor gate current requirements are similar to those for the power bipolar transistor (now virtually obsolete) when reverse base current is used for BJT turn-off. Figure 8.17 shows a gate drive circuit for a GTO thyristor which is similar to that historically used for power bipolar junction transistor base drives. The inductor *L,* in figure 8.17, is the key turn-off component since it controls the *di/dt* of the reverse gate current. The smaller the value of *L,* the larger the reverse *di/dt* and the shorter the turn-off time. But with a shorter turn-off time the turn-off gain decreases, eventually to unity. That is, if the GTO thyristor is switched off rapidly, the reverse gate current must be of the same magnitude as the anode current to be extinguished. A slowly applied reverse gate current *di/dt* can produce a turn-off gain of over 20 but at the expense of increased turn-off saturation delay and switching losses. For the GTO thyristor *L* is finite to get a turn-off gain of more than one, while to achieve unity gain turn-off for the GCT, *L* (which includes stray inductance) is minimised.

The GTO thyristor cathode-to-gate breakdown voltage rating V_{RGM} specifies the maximum negative rail voltage. A level of -15 to -20V is common, and for supply rail simplicity a ± 15 V rail may be selected. Resistor R_4 limits the base current of T_t. If an open collector ttl driver is employed, the current through R_4 is given by

$$I_{OL} = (V_{cc} - V_{beT_t} - V_{Db} - V_{OL}) / R_4 \qquad \text{(A)}$$

For the open collector 74 ttl series, I_{OL} = 40 mA when V_{OL} = 0.5 V whence R_4 can be specified. The resistor R_3 speeds up turn-off of T_t. It is as large as possible to ensure that minimal base current is diverted from T_t. Diodes D_b and D_{as} form a Baker's clamp, preventing T_t from saturating thereby minimising its turn-off delay time.

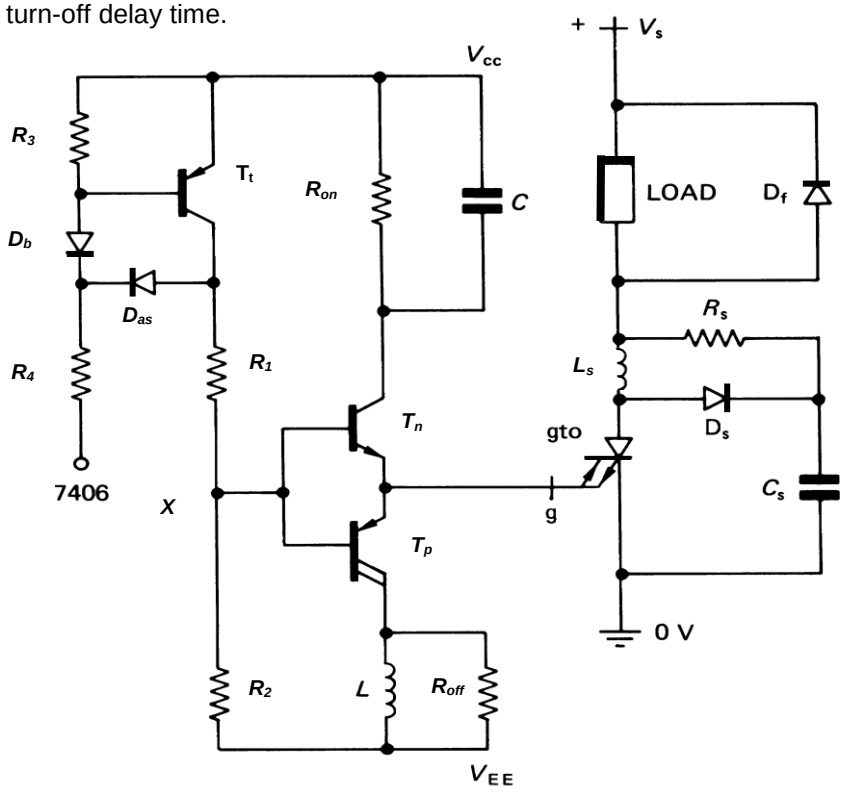


Figure 8.17. *Gate drive circuit and anode snubber circuits for a GTO thyristor.*

The two driver transistors T_n and T_p should

- have high gains
- be fast switching
- have collector voltage ratings in excess of $V_{cc} + V_{EE}$.

The GTO thyristor gate turn-on current is determined by resistor R_{on}, which is specified by

$$R_{on} = \frac{V_{cc} - V_{ceT_n} - V_{GC}}{I_G} \qquad \text{(Ohms)}$$

The power rating of R_{on} is given by

$$P_{R_{on}} = \delta(V_{cc} - V_{ceT_n} - V_{GC})I_G \qquad \text{(W)}$$

where δ is the maximum on-state duty cycle. The capacitor C_{on}, in parallel with R_{on}, provides a short current boost at turn-on, as shown in figure 8.7, thereby speeding up thyristor turn-on, increasing turn-on initial *di/dt* capability, and reducing turn-on losses.

The series resistors R_1 and R_2 bias the bases of the totem pole level shift driver and, for an on-condition, the potential of point X in figure 8.17 is given by

$$V_X = V_{beT_n} + V_{GC} \qquad \text{(V)}$$

The total current flow through R_1 is made up of the transistor T_n base current and that current flowing through R_2, that is

$$I_{R1} = \frac{I_G}{\beta_{T_n}} + \frac{V_X + V_{EE}}{R_2} \qquad \text{(A)}$$

from which

$$R_1 = (V_{cc} - V_X) / I_{R1} \qquad \text{(ohms)}$$

The power rating of R_1 is

$$P_{R_1} = \delta(V_{cc} - V_X)I_{R_1} \qquad \text{(W)}$$

For fast turn-off, if the reverse gate current at turn-off is to be of the same magnitude as the maximum anode current, then R_2 must allow sufficient base current to drive T_p. That is

$$R_2 = \frac{V_X + V_{beT_p}}{I_c / \beta\beta_p} \qquad \text{(ohms)}$$

Once the gate-to-cathode junction of the GTO has recovered, the reverse gate current decays to the leakage level. The power rating of R_2 can be low at lower switching frequencies.

The small inductor L in the turn-off circuit is of the order of microhenrys and it limits the rate of rise of reverse gate current, while R_{off} damps any inductor current oscillation.

The turn-on and turn-off BJT output totem pole in figure 8.17 can be replaced by suitable n-channel MOSFET circuitry in high power GCT and GTO thyristor applications. In high power IGCT applications, MOSFETs and rail decoupling electrolytic capacitors are extensively parallel connected. Typically 21 capacitors and 42 MOSFETs are parallel connected to provide a low impedance path for unity anode current extraction from the GCT gate. The gate inductance (including the GCT internal package inductance) is minimised, whence L is zero. Typically, the IGCT gate drive, gate connection, and internal package inductance are each about 2nH. This is achieved by minimising lengths, capacitive decoupling, and using parallel go and return paths. As a result, gate reverse *di/dt*'s of over 5kA/μs are attainable with a -15V dc negative gate supply.

Table 8.4: Gate drive isolation techniques summary

Technique	data transfer	power transfer	comments
Transformer	direct signal coupling	direct magnetic transfer	duty cycle limited corona breakdown limit
opto-coupler	slow, with capacitive effects	n/a	voltage and *dv/dt* limit
fibre optics	fast, virtually no voltage limit	n/a	best signal transmission at MV and HV
charge couple	n/a	requires switching	induced effects between ground level and gate level, LV application
bootstrap	n/a	requires switching	

Reading list

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Problems

8.1. Calculate suitable resistor values for the triac gate drive circuit in figure 8.8a, assuming a minimum gate current requirement of 50 mA and the gain of Q1 is 50 at 50 mA.

8.2. Repeat problem 8.1 for the circuits in figures
- 8.8b
- 8.8c
- 8.8d.

8.3. Repeat example 8.2 assuming a 2V triac gate threshold voltage for turn-on.