CHAPTER 5

Cooling of Power Switching Semiconductor Devices

Semiconductor power losses are dissipated in the form of heat, which must be transferred away from the switching junction, if efficient switching is to be maintained. The reliability and life expectancy of any power semiconductor are directly related to the maximum device junction temperature experienced. It is therefore essential that the thermal design determine accurately the maximum junction temperature from the device power dissipation. Every 10°C junction temperature decrease, doubles device lifetime.

i. Heat load

The heat load may be active or passive, then there is a combination of the two. An active load is the heat dissipated by the device being cooled. It is generally equal to the input power to the device, for example, $P = V \times I = I^2 \times R = V^2 / R$. Passive heat loads are indirect, are parasitic in nature, and may consist of radiation, convection or conduction.

Heat energy, due to a temperature difference, can be transferred by any of, or a combination of, three mechanisms, viz.,

- Convection - heat transferred to a moving fluid which takes the heat away
- Conduction - heat flows through a thermal conducting material, away from the heat source
- Radiation - heat flow by long-wave electromagnetic radiation, e.g. infrared.

Electromagnetic thermal *radiation* heat transfer

When two objects at different temperatures come within proximity of each other, heat is exchanged between them. Electromagnetic wave propagation, radiation is emitted from one object and absorbed by the other. As a result of the temperature difference, the hot object experiences a net heat loss and the cold object undergoes a net heat gain. This is termed *thermal radiation*.

Radiation heat loads are usually considered insignificant when the system is operated in a gaseous environment since other passive heat loads are usually greater. Radiation loading is usually significant in systems with small active loads and large temperature differences, especially when operating in a vacuum environment, where convection processes are absent.

Electromagnetic thermal ***radiation*** heat loading (for a grey body, $\varepsilon < 1$) is given by

$$P_d = \sigma \varepsilon A (T_1^4 - T_2^4) \qquad (5.1)$$

where P_d is the rate of radiated heat transfer (that is, the power dissipated), W
σ is the Stefan-Boltzmann constant (5.667×10^{-8} W/m^{2}K^4)
ε is a surface property, termed emissivity, $0 \le \varepsilon \le 1$, see Table 5.6 and Appendix 5.11
A is the surface area involved in the heat transfer, m^2
T is absolute temperature, K

The ideal emitter, or black body, is one which gives off radiant energy with $\varepsilon = 1$ in equation (5.1).

Conduction **heat transfer**
Conductive heat transfer occurs when energy exchange takes place, by direct impact of molecules, from a high temperature region to a low temperature region.
Conductive heat loading on a system may occur through lead wires, mounting screws, etc., which form a thermal path from the device being cooled to the heat sink or ambient environment.

The one-dimensional model for general molecular (non-radiation) heat transfer is given by

$$P_d = -\lambda A \frac{\delta T}{\delta \ell} + \rho_m A \ell \frac{\delta T}{\delta t} \quad \text{(W)} \tag{5.2}$$

where $\delta T = T_2 - T_1$ or ΔT, is the temperature difference between two regions of heat transfer
λ is thermal conductivity, W/m K, see Appendix 5.11
ρ_m is density of the heatsink material
c_p is specific heat capacity, J/kg K, such that $\Delta T = W/mc_p$ (W is energy, m is mass)
ℓ is distance (thickness).
Equation (5.2) shows that the thermal power generated P_d is balanced by the stored thermal power (first term on the right hand side) and the thermally dissipated power (second term on the right hand side).

Assuming steady-state heat dissipation conditions, then $\delta T / \delta t = 0$ in equation (5.2).

Conduction through a homogeneous solid, from Fourier's law of heat conduction, is therefore given by

$$P_d = \lambda A \frac{dT}{dx} = \frac{\lambda}{\ell} A \Delta T \quad \text{(W)} \tag{5.3}$$

Convection **heat transfer**
When the temperature of a fluid (a gas or liquid) flowing over a solid object differs from that of the object surface, heat transfer occurs. The amount of heat transfer varies depending on the fluid flow rate. Convective heat loads are generally a result of natural (or free) convection. This is the case when gas flow is not artificially created as by a fan or pump (forced convection), but rather occurs naturally from the varying density in the gas caused by the temperature difference between the object being cooled and the gas. Heat transfer processes that involve *change of phase* of a fluid (for example evaporation or condensation) are also considered to be convection.
The convective loading is a function of the exposed area and the difference in temperature between the load and the surrounding gas. Convective loading is usually most significant in systems operating in a gaseous environment with small active loads or large temperature differences.

Convection heat transfer through a fluid or air, under steady-state conditions in equation (5.2), is given by Newton's law of cooling, that is

$$P_d = h A \Delta T \quad \text{(W)} \tag{5.4}$$

The convection heat transfer coefficient h $(= \lambda / \ell)$, W/m^{2}K, depends on the heat transfer mechanism used and various factors involved in that particular mechanism. It is not a property of the fluid.
Natural or *free convection* is essentially still to slightly stirred air with h values ranging from 1 to 25. *Forced convection* is air moved by a fan or other active method, giving h values ranging from 10 to 100. Values for forced liquid convection are 50 to 20,000, while the h range for boiling and condensation is 2,500 to 100,000.

For natural vertical convection in free air, the losses for a plane surface may be approximated by the following empirical formula

$$P_d = 1.35 A \sqrt[4]{\frac{\Delta T^5}{\ell}} = 1.35 A \sqrt[4]{\frac{\Delta T}{\ell}} \Delta T = hA\Delta T \quad \text{(W)} \tag{5.5}$$

where ℓ is the vertical height in the direction of the airflow and h is of the form

$$h = K \left(\frac{\Delta T}{\ell} \right)^{1/4} \tag{5.6}$$

Two cases occur for forced airflow, and the empirical losses are

- *for laminar flow*

$$P_d = h A \Delta T = 3.9 \sqrt{\frac{v}{\ell}} A \Delta T \quad \text{(W)} \tag{5.7}$$

- *for turbulent flow*

$$P_d = h A \Delta T = 6.0 \sqrt[5]{\frac{v^4}{\ell}} A \Delta T \quad \text{(W)} \tag{5.8}$$

where v is the velocity of the vertical airflow.

Combined *convection* and *conduction* heat transfer

Heat Loss (or gain) - through the walls of an insulated container (combined convection and conduction, estimation) is

$$P_d = A \times \frac{\Delta T}{\ell / \lambda + 1/h}$$

where P_d is the heat lost or gained, W
ℓ is the thickness of insulation, m
λ is the thermal conductivity of the insulation material, W/m K
A is the outside surface area of the container, m^2.
h is the convection heat transfer coefficient of the surface material, W/m^2 K
$\Delta T = T_{o/s} - T_{i/s}$
$T_{o/s}$ is the outside temperature, °C
$T_{i/s}$ is the inside temperature, °C

ii. Transient heating

Some designs require a set amount of time to reach the desired temperature.
The estimated time required to heat (or cool) an object (also known as Newton's Law of Cooling) is

$$t = \frac{m \times c_p \times \Delta T}{P}$$

P is the mean heat added (or being removed) from the object, W, watts
m is the mass (weight) of the object, kg (density x volume)
c_p is the specific heat of the object material, J/kg K
t is the time required to cool down (or heat up) the object in seconds
$\Delta T = T_o - T_f$
T_o is the starting temperature, °C
T_f is the final temperature, °C

$$P = ½\left(P_{t_o} + P_{t_t}\right)$$

P_{to} is the initial heat pumping capacity when the temperature difference across the cooler is zero.
P_{tt} is the heat pumping capacity when the desired temperature difference is reached and heat-pumping capacity is decreased.
Heat loading may occur through one or more of four modes: active, radiation, convection or conduction. By utilizing these equations, the heat load can be estimated.

iii. Thermal resistance

It is generally more convenient to work in terms of thermal resistance, which is defined as the ratio of temperature change to power. Thermal capacity is the reciprocal of thermal resistance. For conduction, from equation (5.4), thermal resistance R_θ is

$$R_\theta = \frac{\Delta T}{P_d} = \frac{1}{hA} = \frac{\ell}{\lambda A} \quad \text{(K/W)} \tag{5.9}$$

where the conduction thermal heat transfer coefficient, h, is

$$h = \frac{\lambda}{\ell} \tag{5.10}$$

The average power dissipation P_d and maximum junction temperature $\hat{T}_j$, in conjunction with the ambient temperature T_a, determine the necessary heat sink, according to equation (5.9)

$$P_d = \frac{\Delta T}{R_{\theta \text{j-a}}} = \frac{\hat{T}_j - T_a}{R_{\theta \text{j-a}}} \quad \text{(W)} \tag{5.11}$$

where $R_{\theta \text{j-a}}$ is the total thermal resistance from the junction to the ambient air. The device user is restricted by the thermal properties from the junction to the case for a particular package, material, and header mount according to

$$P_d = \frac{\Delta T}{R_{\theta \text{j-c}}} = \frac{\hat{T}_j - T_c}{R_{\theta \text{j-c}}} \quad \text{(W)} \tag{5.12}$$

where T_c is the case temperature, K and
$R_{\theta \text{ j-c}}$ is the package junction-to-case mounting thermal resistance, K/W.

An analogy between the thermal (and magnetic) equations and Ohm's law and Kirchhoff's laws is often made to form models of heat flow. The temperature difference ΔT could be thought of as a voltage drop ΔV, thermal resistance R_θ corresponds to electrical resistance R, and power dissipation P_d is analogous to electrical current I. *[viz.,* $\Delta T = P_d R_\theta \equiv \Delta V = IR$*].* See Table 5.10.

For convection, from equation (5.4), the effective thermal resistance is

$$R_\theta = \frac{\Delta T}{P_d} = \frac{1}{hA} \tag{5.13}$$

For radiation, from equation (5.1), the effective thermal resistance of radiation is

$$R_\theta = \frac{\Delta T}{P_d} = \frac{1}{\sigma\varepsilon A \times (T_1 + T_2)(T_1^2 + T_2^2)} = \frac{1}{h_r A} \tag{5.14}$$

where the radiation heat transfer coefficient, h_r, in W/m^{2}K, is

$$h_r = \sigma\varepsilon \times (T_1 + T_2)(T_1^2 + T_2^2) \approx 4 \times \sigma\varepsilon \times T_{mean}^3 \tag{5.15}$$

where T_{mean} is the arithmetic mean of T_1 and T_2, specifically ½($T_1 + T_2$).

5.1 Thermal resistances

A general thermal dissipation model or thermal equivalent circuit for a mounted semiconductor is shown in figure 5.1. The total thermal resistance from the virtual junction to the open air (ambient), $R_{\theta\,\text{j-a}}$, is

$$R_{\theta\text{j-a}} = R_{\theta\text{j-c}} + \frac{R_{\theta\text{c-a}} \times (R_{\theta\text{c-s}} + R_{\theta\text{c-a}})}{R_{\theta\text{c-a}} + R_{\theta\text{c-s}} + R_{\theta\text{s-a}}} \quad \text{(K/W)} \tag{5.16}$$

In applications where the average power dissipation is of the order of a watt or so, power semiconductors can be mounted with little or no heat sinking, whence

$$R_{\theta\text{j-a}} = R_{\theta\text{j-c}} + R_{\theta\text{c-a}} \quad \text{(K/W)} \tag{5.17}$$

Generally, when employing heat sinking, $R_{\theta\,\text{c-a}}$ is large compared with the other model components and equation (5.16) can be simplified to three series components:

$$R_{\theta\text{j-a}} = R_{\theta\text{j-c}} + R_{\theta\text{c-s}} + R_{\theta\text{s-a}} \quad \text{(K/W)} \tag{5.18}$$

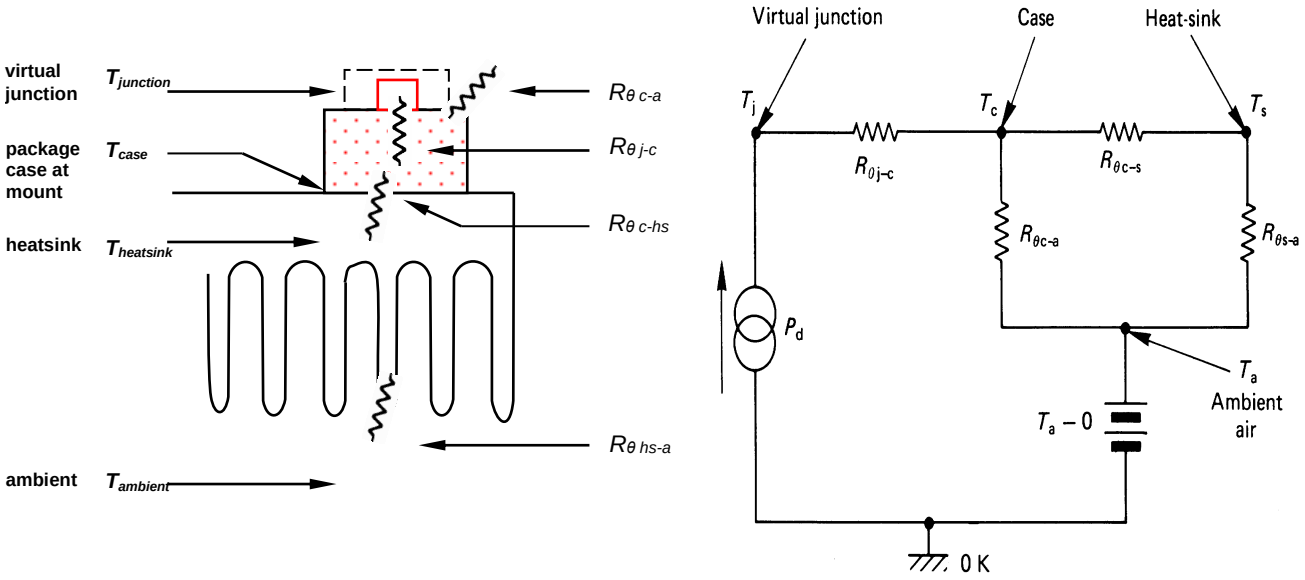

Figure 5.1. *Semiconductor thermal dissipation equivalent circuit.*

5.2 Contact thermal resistance, $R_{\theta\,c\text{-}s}$

The case-to-heat-sink thermal resistance $R_{\theta\,\text{c-s}}$ (case means the device thermal mounting interface surface) depends on the package type, interface flatness and finish, mounting pressure, and whether thermal-conducting grease and/or an insulating material (thermal interface material, TIM) is used. In general, increased mounting pressure decreases the interface thermal resistance, and no insulation other than thermal grease results in minimum $R_{\theta\,\text{c-s}}$. Common electrical insulators are mica, aluminium oxide, and beryllium oxide in descending order of thermal resistance, for a given thickness and area. Table 5.1 shows typical contact thermal resistance values for smaller power device packages, with various insulating and silicone grease conditions. Silicon based greases are best, for example Assmann V6515, spread at a thickness of 100µm to 150µm, on both surfaces. Grease in excess of this will be squeezed out under clamping pressure. Initial grease thermal resistance decreases slightly after a few normal deep thermal cycles.

Table 5.1: Typical case-to-heat-sink thermal resistance value for various small packages

Package	*Insulating washer*	$R_{\theta c\text{-}s}$ (K / W)	
		Silicone grease	
		with	*without*
TO-3	No insulating washer	0.10	0.3
	Teflon	0.7-0.8	1.25-1.45
	Mica (50 - 100 μm)	0.5-0.7	1.2-1.5
TO-220	No insulating washer	0.3-0.5	1.5-2.0
	Mica (50 - 100 μm)	2.0-2.5	4.0-6.0
TO-247	No insulating washer	0.1-0.2	0.4-1.0
	Mica (50 - 100 μm)	0.5-0.7	1.2-1.5
SOT-227 ISOTOP	No insulating washer	0.1-0.2	0.3-0.4
	Mica (50 - 100 μm)	0.5-0.7	1.0-1.2

The thermal resistance of a heat-conducting layer is inversely proportion to heat conductivity of the material and in direct ratio to its thickness. If the clamping pressure is increased, the layer thermal resistance falls. In figure 5.2, the exemplary dependence of the gasket thermal resistance per surface unit on pressure is shown. However, with a growth of pressure it is necessary to find an optimum, as the clamping effort should not exceed a package recommended value or introduce differential thermal expansion problems into the clamping arrangement.

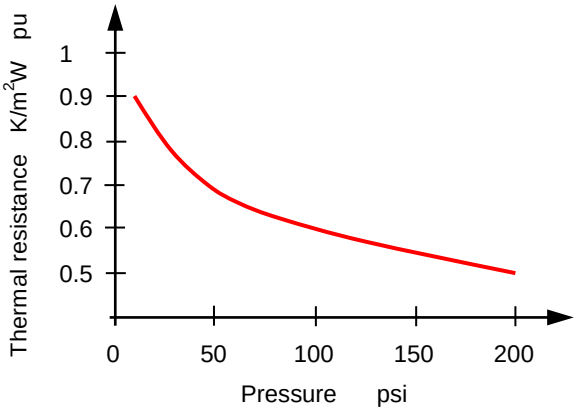

Figure 5.2. *Exemplary dependence of the gasket thermal resistance on clamping pressure.*

5.2.1 Thermal interface materials

To be effective, heatsinks require intimate surface-to-surface contact with the component to be cooled. Unfortunately, irregular surface areas, both on the electronic components and on the heatsink mating surface prevent good contact. Up to 99% of the surfaces are separated by a layer of interstitial air, which is a poor conductor of heat thus presents a thermal barrier. Therefore, a thermally conductive interface material is necessary to fill the interstices and microvoids between the mating surfaces. To ensure that electrical problems are not inadvertently introduced while solving the thermal problems, it is often essential that the thermal interface materials also perform an electrical isolation function. Thermal interface materials TIMs vary widely in terms of performance (that is, thermal, electrical, and physical properties), general appearance, and mode of application. Among the most commonly used classes of thermal interface materials are: thermal greases, cure-in-place thermally conductive compounds, gap filling thermally conductive elastomeric pads, thermally conductive adhesive tapes, and phase change materials, all of which are summarised in Table 5.2 and are briefly described.

- Thermal Greases
  Comprised of thermally conductive ceramic fillers in silicone or hydrocarbon (organic) oils, as shown in Tables 5.3a and b, a thermal grease is a paste, which is applied to at least one of the two mating surfaces. When the surfaces are pressed together, the grease spreads to fill the void. During compression, excess grease squeezes out from between the mated surfaces. Some form of clip or other mounting hardware is needed to secure the joint. Although it is comparatively inexpensive and thermally effective, thermal grease is not an electrical insulator. Disadvantageously, it can be inconvenient to dispense and apply, and requires cleanup to prevent contamination problems.

- Cure-in-Place Thermally Conductive Compounds
  A thermally conductive compound again incorporates thermally conductive ceramic fillers, shown in Table 5.3, but unlike thermal greases, the binder is a rubber material. When first applied, the paste-like compound flows into the interstices between the mating surfaces. Then, when subjected to heat, it cures into a dry rubber film. Besides its thermal properties, this film also serves as an adhesive, allowing a tight, void-free joint without the need for additional fasteners. Thermally conductive compounds can fill larger gaps in situations where thermal greases might ooze from the joint. Although application and performance is similar to that of thermal grease, cleanup is easier, simply involving removal of the excess cured rubber film.

- Thermally Conductive Elastomeric Pads
  A thermally conductive elastomeric pad consists of a silicone elastomer filled with thermally conductive ceramic particles and may incorporate woven glass fibre or dielectric film reinforcement. Typically ranging in thickness from 0.1 to 5 mm and in hardness from 5 to 85 Shore A, these pads provide both electrical insulation and thermal conductivity, making them useful in applications requiring electrical isolation. Thicker pads prove useful when large gaps must be filled. During application, the pads are compressed between the mating surfaces to make them conform to surface irregularities. Mounting pressure must be adjusted according to the hardness of the elastomer to ensure that voids are filled. A mechanical fastener is essential to maintain the joint once assembled.

- Thermally Conductive Adhesive Tapes
  A thermally conductive adhesive tape is a double-sided pressure sensitive adhesive film filled with thermally conductive ceramic powder. To facilitate handling, aluminium foil or a polyamide film may support the tape; the latter material also provides electrical insulation. When applied between mating surfaces, the tape must be subjected to pressure to conform to the surfaces. Once the joint is made, the adhesive holds it together permanently, eliminating the need for supplemental fasteners. No bond curing is needed. One limitation of thermally conductive tapes is that they cannot fill large gaps between mating surfaces as well as liquids; hence, the convenience of tape mounting is traded against a nominal sacrifice in thermal performance.

- Phase Change Materials
  Solid at room temperature, phase change materials, shown in Table 5.3, melt (that is, undergo a phase change) as the temperature rises to the 40° to 70°C range. This makes the material (0.13 mm thick in its dry film form) as easy to handle as a pad, while assuring, when subjected to heat during the assembly process, the melt flows into voids between mating surfaces as effectively as a thermal grease. Applying power to the power electronic component introduces the needed heat for the phase change to occur, establishing a stable thermal joint. These materials consist of organic binders (that is, a polymer and a low-melt-point crystalline component, such as a wax), thermally conductive ceramic fillers, and, if necessary, a supporting substrate, such as aluminium foil or woven glass mesh. See section 5.2.2 for further details.

Table 5.2: Thermal Interface Material (TIM) thermal resistances

Interface	Thickness mm	Thermal Conductivity λ W / m.K	Thermal resistance $R_{\theta c\text{-}s}$ K / W	Thermal resistance pu area K cm^2/W
Dry Joint	n/a	n/a	2.9	1.8 - 2
Thermal Grease	0.076	0.7	0.9	0.5 - 1.1
Thermal Compound	0.127	1.2	0.8	0.2 - 0.7
Elastomer	0.254	5.0	1.8	1 - 2
Adhesive Tape	0.229	0.7	2.7	0.5 - 1.5
Eutectic (soldering) Sn(91) Zn(9)		61		0.1

Table 5.3: Thermal Interface material (TIM) parameters

Material parameters	Thermal Conductivity	Resistivity	Temperature range	Thickness		Lifetime
(a) Thermal grease	λ, W / mK	ρ, Ω.cm	°C	mm		
Zinc Oxide/Silicone	0.74	> 5×10^{14}	< 150			5 years @ 25C
$A\ell_20_3$ / Non-Silicone	2	> 10^{13}	< 150			1 year @ 25°C
AℓN / Non-Silicone	4	> 10^{13}	< 150			1 year @ 25°C
Non-silicone paste	2	> 1×10^{13}	n/a			1 year @ 25°C
Silicone paste	> 4.0	> 1×10^{14}	n/a			1 year @ 25°C
Non-curing paste	4	> 1×10^{13}	n/a			n/a
Non-silicon polysynthetic oils	> 7.5	1Å	-50…+150			n/a
thermal phase change	0.90	1×10^{14}	-50…+200			n/a
Silicone	0.8-1.2	1×10^{13}	-60…+180			5 years
(b) Heat conducting gaskets					Tensile Strength psi	
Silicon/Alumina filled	0.38	1×10^{14}	-60…+150	0,08	3000	
Silicon/Boron Nitride	2.07	1×10^{14}	-60…+200	0,25	1000	
$A\ell_2O_3$ filled	1.7	n/a	< +150	0,10	15…300	
AℓN filled	3.6	n/a	< +150	0,10	15…300	
97% Graphite filled	5	n/a	< +450	0,13	15…300	
(c) Phase changing heat conducting gaskets					Clamping psi	Phase Change Temperature °C
Black/self-adhesive layer	0.7	n/a	< +120	0.077	10…200	< +120
Grey/self-adhesive layer	1.0	5×10^{15}	-60…+125	0.13	20…60	-60…+125
Grey/self-adhesive layer	0.6	5×10^{14}	-60…+125	0.18	50…300	-60…+125
Grey/self-adhesive layer	3	n/a	n/a	0.11	n/a	n/a

5.2.2 Phase change gasket materials (solid to liquid)

The inavertable heat produced by power electronics necessitates a carefully designed thermal path along which all of the thermal resistances are minimized. For the case-to-heatsink interface, this requires that thermal grease be used to minimize the interface resistance. Phase change materials, PCMs, are an alternative to the messy application and migration problems associated with thermal grease.

The term *phase change* describes a class of materials that are solid at room temperature and change to a liquid as temperature increases. This phase change, or melting, occurs in the range of 40 to 70°C. PCMs are composed of a mixture of organic binders, fine particle ceramic fillers for thermal enhancement, and, optionally, a supporting substrate, such as aluminium foil or a woven glass mesh. The organic binder is a blend of a polymer and a low-melt-point crystalline component, such as a wax. The ceramic fillers may be $A\ell_20_3$, BN, AℓN or Zn0.

The way a PCM performs compared to a dry interface joint and thermal grease is illustrated in figure 5.3, where the case to heatsink temperature difference is plotted against elapsed time after the commencement of power dissipated. The curve representing the dry interface shows rapid thermal equilibrium at about 13°C. The curve involving the use of thermal grease shows the same rapid rise to thermal steady-state but at a lower temperature difference of 4°C. The thermal grease significantly reduces the interface resistance by eliminating the interstitial air.

The PCM - a 0.1 mm thick dry film - behaves as a combination of the two interfaces. Initially at power up, the cool components give the dry interface behaviour, with the temperature difference rapidly increasing to about 12°C. As the system temperature increases, the PCM melts and the clamping pressure exerted by the clamping mechanism forces the liquid to spread in the thermal joint. As the liquid spreads, the molten

PCM displaces the interstitial air and the distance between the surfaces decreases. Both of these processes act to reduce the thermal resistance of the interface and the temperature difference is seen to decrease rapidly, reaching the performance of thermal grease, 4°C. In effect, the solid PCM film has turned into thermal grease and a grease-like joint has been formed. The next time the thermal load is activated, the interface does not experience the large temperature difference because the void free thermal joint has already been established.

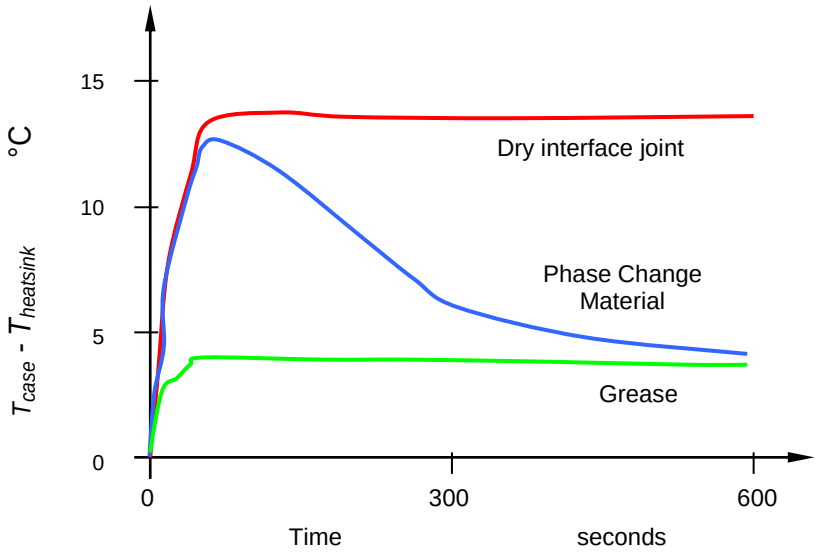

Figure 5.3. *Performance of a PCM, compared to a dry interface joint and thermal grease.*

The thermal resistance across an interface depends on the thermal conductivity of the PCM in the interface and its conductive path length. Thermal conductivity is a function of the type and level of the ceramic filler in the formulation, typically between 0.7 and 1.5 W/m.K. The amount of filler that can be added is limited by the need to keep the viscosity as low as possible to achieve proper flow of the PCM in the interface. The thickness of the interface formed by a PCM is determined by the flatness of the mating surfaces, the clamping pressure, and the viscosity and rheology of the molten PCM. Most commercial surfaces deviate from true flatness by as much as 2µm/mm. This means that the thermal path between a module surface and the heatsink may be as much as 100µm, and more with large heatsinks. Critical applications may require a better surface flatness through additional machining operations to reduce the thermal path.

The viscosity and the rheology of the PCM above its melt point represent another factor determining the thickness of the interface. As the PCM melts in the interface, the pressure applied by the mounting clamps forces the liquid to spread, eliminating the interstitial air and allowing the space between the two surfaces to decease. If the viscosity is high, the low force of the clamps will be insufficient to cause sufficient spreading and the conduction path will be long. Low viscosity on the other hand will allow the liquid to fill most of the joint, resulting in the thinnest joint. Using a stronger mounting force will aid the spreading process, but there is a package limit as to the amount of pressure that can be applied.

Phase change materials offer the same thermal performance as thermal grease without the mess and contamination associated with grease. They can be supplied attached to a heatsink as a dry film. As soon as they are heated above their phase change temperature, they melt and perform as well as, or often better than, thermal grease. Once this interface has been formed, it remains stable until the sink is physically separated from the power module case-mounting surface.

5.3 Heat-sinking thermal resistance, $R_{\theta\,s\text{-}a}$

The thermal resistance for a flat square plate heat sink may be approximated by

$$R_{\theta s\text{-}a} = \frac{3.3}{\sqrt{\lambda\, b}} C_f^{1/4} + \frac{650}{A} C_f \qquad \text{(K/W)} \qquad (5.19)$$

Typical values of heatsink thermal conductance λ in W/K cm at 350 K, are shown in Appendix 5.11 and

b is the thickness of the heat sink, mm

A is the area of the heat sink, cm^2

C_f is a correction factor for the position and surface emissivity of the heat-sink orientation according to Table 5.4.

Table 5.4: Heatsink correction factor

Surface position C_f	shiny	blackened
vertical	0.85	0.43
horizontal	1.0	0.5

Table 5.5: Fin spacing versus flow and fin length

Fin length (mm) H	75	150	225	300
Airflow (m/s) v	Fin Spacing (mm) s			
natural convection	6.5	7.5	10	13
1.0	4.0	5.0	6.0	7.0
2.5	2.5	3.3	4.0	5.0
5.0	2.0	2.5	3.0	3.5

Table 5.6: Emissivity coefficient of various surface treatments at 100°C

Surface	Emissivity ε
Polished aluminium	0.05
Polished copper	0.07
Rolled sheet steel	0.66
Oxidised copper	0.70
Black anodised aluminium	0.70 - 0.90
Black air-drying enamel	0.85 - 0.91
Dark varnish	0.89 - 0.93
Black oil (organic) paint	0.92 - 0.96
Al_2O_3	0.15

The correction factor C_f illustrates the fact that black surfaces are better heat radiators and that warm air rises, creating a 'chimney' effect. Equation (5.19) is valid for one power-dissipating device, in the centre of the sink, at a static ambient temperature up to about 45°C, without other radiators in the near vicinity.
In order to decrease thermal resistance, inferred by equation (5.9), finned-type heat sinks are employed which increase sink surface area. Figure 5.6 illustrates graphs of thermal performance against length for a typical aluminium finned heat sink. This figure shows that $R_{\theta\,s\text{-}a}$ decreases with increased sink length.

If the fin thickness, t, is small relative to the fin spacing, s, the following equation can be used for estimating the thermal resistance of a vertical heat sink in natural convection.

$$R_{\theta hs-a} = \frac{1}{h \times \text{total fin area}} = \frac{1}{h \times (2n_f LH)} \qquad (5.20)$$

where a fin efficiency of unity has been assumed (see equation (5.22)) and the number of fins, n_f, is

$$n_f = \frac{W_{hs}}{s + t}$$

Minimal thermal reduction results from excessively increasing base length, H, as shown in figure 5.6b. The maximum distance between fins, s, depends on the fin depth, L, and width of the fins, t, with deep finned heat sinks needing more space between adjacent fins than a shallow design, unless fan cooling is used. The minimum spacing s is determined by fin depth, L, and airflow. If the fins are packed too closely, the flow through them is significantly reduced and therefore the heat transfer coefficient, h, decreases. The deeper the fins, L, the more space needed between them since a portion of the heat is radiated to adjacent fins, which helps to stabilise the temperature, but does little to dispose of the heat (in figure 5.4a, about 30% of the heat is radiation transferred fin-to-fin, hence not all dissipated).

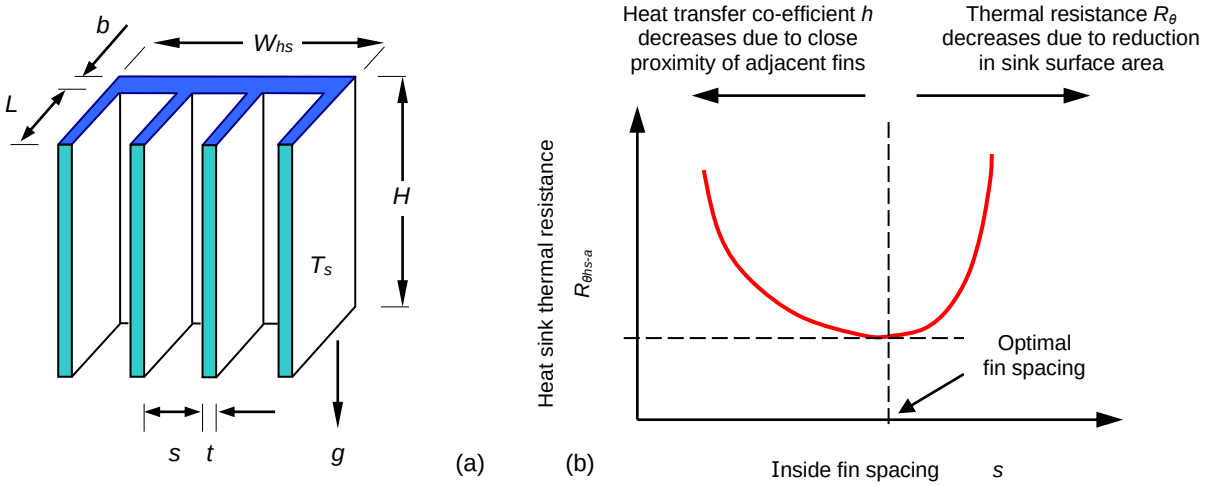

Figure 5.4. *Heat sink dimension parameters and thermal resistance dependence on fin spacing.*

As the base flow height H is increased, the air at the top of a vertical heatsink is hotter than that entering at the bottom. If the fin depth L is increased, there is more mutual radiation between fins, and as the spacing is reduced, mutual radiation increases further. Airflow is also restricted because of the smaller physical area for air to pass, since more of the available space is occupied by the heatsink itself.
The performance of a heatsink is linearly proportional to the base width W_{hs} of the sink in the direction perpendicular to the flow and proportional to the square root of the fin base length H in the direction of the airflow. (The heat transfer coefficient h is inversely related to H). Therefore it is better to increase the width rather than the length, provided the width is not already excessive compared to the length.

Heat transfer coefficient h can be defined in a number of ways. If it is defined referenced to the inlet fluid temperature of the heatsink, the heatsink thermal resistance is calculated by

$$R_{\theta hs-a} = \frac{1}{\eta_f h A} \tag{5.21}$$

where A is the total surface area of fins and base between fins and
η_f is the fin efficiency, defined as

$$\eta_f = \frac{\tanh(m_f \times H)}{m_f \times H} \quad \text{in which} \quad m_f = \sqrt{\frac{h \times P_{\square}}{\lambda \times A_x}} \tag{5.22}$$

where H is the base height of the fin, m
$P_{\square}$ is the fin perimeter, m
A_x is the fin cross sectional area, m^2
m_f is the mass flow rate, equal to $\rho_\ell \times V_f \times s \times L$, kg/s
ρ_ℓ fluid density (= 1/v specific volume), kg/m^3
V_f is the velocity between the fins
If the heat transfer coefficient is defined based on the temperature between the fins, the thermal resistance expression involves a heat capacitance component:

$$R_{\theta hs-a} = \frac{1}{\eta h A} + \frac{1}{2 m_f c_p} \tag{5.23}$$

where c_p is the fluid specific heat capacitance at constant pressure, kJ/kg.K.

Estimating radiation heat transfer from an extruded heat sink
The effect of radiation heat transfer (hence emissivity, ε) is important in natural convection, as it can be responsible for up to 40% of the total heat dissipation. Unless the heatsink is facing a hotter surface nearby, it is imperative to have the heat sink surfaces thinly painted or correctly anodised to enhance radiation. In natural convection situations where the convective heat transfer coefficient is relatively low, based on the dimensional parameters in figure 5.4a, the radiation heat transfer from all surfaces of the extruded heat sink can be calculated using

$$R_{\theta hs-a} = \frac{1}{\left\{(n_f - 1)\varepsilon_a s + \varepsilon_a \left[n_f t + 2(L + B)\right]\right\} H \sigma (T_s + T_A)(T_s^2 + T_A^2)} \tag{5.24}$$

where n_f is the number of fins
ε_a is the apparent emissivity of a channel
T_s is the heatsink surface temperature and
T_A is the ambient temperature

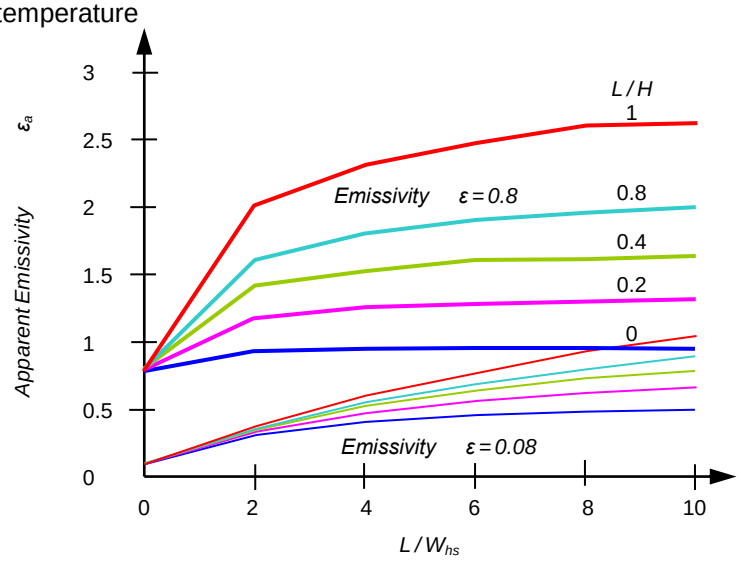

Figure 5.5. *Apparent emissivity ε_a of a channel heatsink of two different surface emissivities for different number of fins and dimensions.*

The apparent emissivity is a function of heat sink dimensions and surface emittances of the sink material, as shown in figure 5.5, for two values of the surface emissivity, namely ε equals 0.08 and 0.8. The apparent emissivity ε_a is based on enclosure theory and assumes a diffused grey surface and constant surface temperature.

The emissivity coefficient, ε, indicates the radiation of heat from a body according the Stefan-Boltzmann law, compared with the heat radiation from an ideal black body where the emissivity coefficient is $\varepsilon = 1$. Regardless of the composition of the emitting surface, the microscopic (and macroscopic) roughness of the surface causes differences in emissivity because a rougher surface has a larger emitting area. Generally, the emissivity of most opaque emitting surfaces increases as wavelength becomes shorter. The emissivity coefficient, ε, for some common surface qualities of aluminium and copper can be found in the Table 5.6 and in Appendix 5.11.
The low emissivity coefficients of untreated, polished aluminium and copper means they have surface finishes that limit the radiated heat from a body. Two thin coats of flat white Krylon #1502 (or equivalent) which has an emissivity of 0.96, should be used on all untreated (emissivity-wise) areas.

Unless otherwise stated, the heat sink is assumed anodised black (emissivity of up to 0.97) and vertically mounted with negligible thermal resistance from case to sink. In accordance with the data in Table 5.4, a general derating of 10 to 15 per cent for a bright surface and 15 to 20 per cent in the case of a horizontal mounting position, are usually adopted. Figure 5.6b also shows the improvement effects on dissipation due to the high thermal conductivity (heat spreader effect) of oxidised copper.

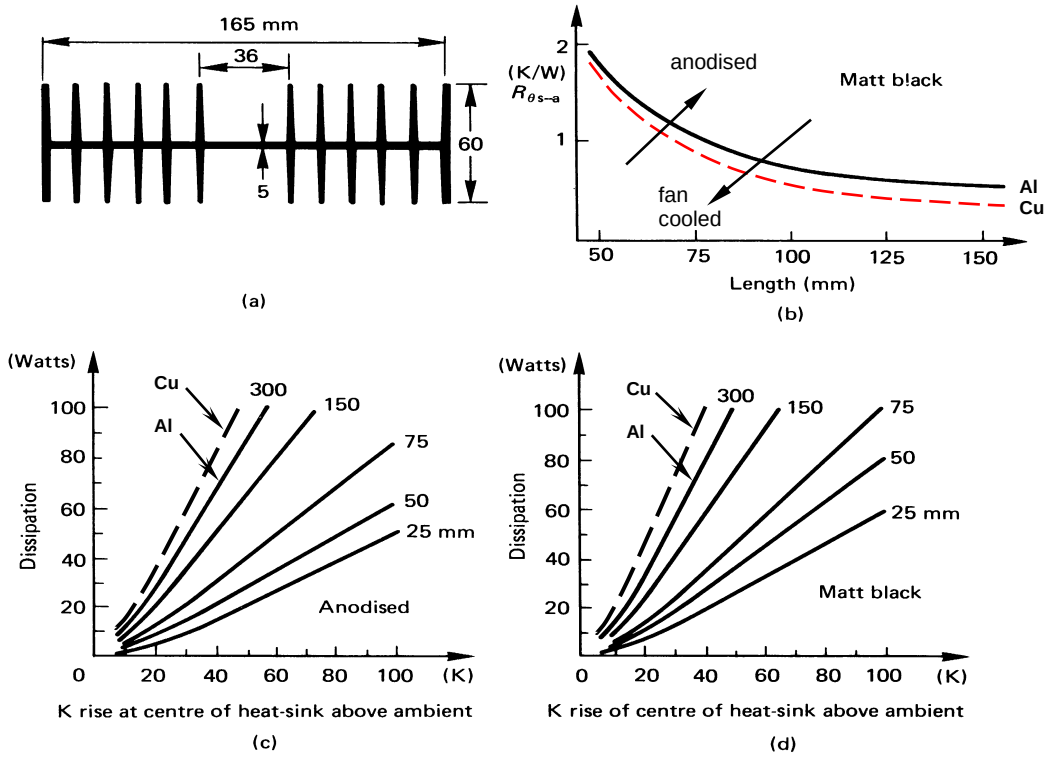

Figure 5.6. *Heat-sink typical data (for aluminium and copper):*
(a) cross-section view; (b) heat-sink length versus thermal resistance for a matt black surface finish;
(c) temperature rise versus dissipation for an anodised finish and different lengths; and
(d) as for (c) but with a matt black surface finish.

Thermal resistance increases with altitude, *z,* above sea level, as air density decreases, according to $R_\theta(z) = R_{O\,metres} / \left(1 - 5 \times 10^{-5} z\right)$. For example: a 1°C/W heatsink degrades to 1.11°C/W at an altitude of 2,000 metres, or 1.18° C/W at 3,000 metres.

The effective sink thermal resistance can be significantly reduced by *forced air cooling*, as indicated in Table 5.5, figure 5.7 and by equations (5.7) and (5.8). If the airflow is

- laminar, heat loss is proportional to the square root of air velocity, equation (5.7);
- turbulent, heat loss is proportional to velocity to the power of 0.8, equation (5.8).

When heatsinks (dissipating a total power of P_{Dtotal}) are vertically stack to share the same vertical natural convention airflow, the air temperature of the flow at the upper heatsink, after passing *n-1* heatsinks, is

$$T_{air} = T_{amb} + \frac{n-1}{n} \frac{c\,v}{P_{D\,total}} \qquad (5.25)$$

The chimney effect results in an airflow velocity *v*, which increases further up the heatsink stack. This and the air density increase results in the upper heatsink being the coolest, even though the passing air is the warmest.

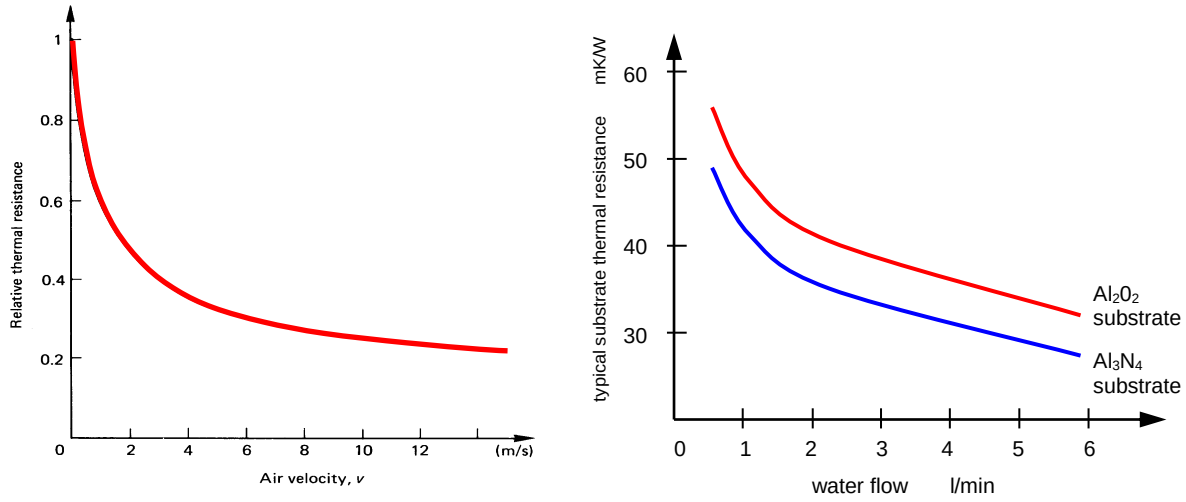

Figure 5.7. *Improved cooling with:*
(a) forced air cooled heat-sink - relative thermal resistance improvement with surface airflow and
(b) thermal resistance dependence on liquid cooling flow rate and substrate material.

5.4 Modes of power dissipation

For long, >1ms, high duty cycle pulses the peak junction temperature is nearly equal to the average junction temperature. Fortunately, in many applications, a calculation of the average junction temperature is sufficient and the concept of *thermal resistance* is valid.
Other applications, notably switches driving highly reactive loads, may create severe current-crowding conditions which render the traditional concepts of thermal design invalid. In these cases, transistor safe operating area or thyristor *di/dt* limits must be observed, as applicable.

In yet other applications, heat cycling can cause power module faults, hence device failure, due to

- thermal cycling – is associated with large base plate (case) temperature changes, ΔT_c
- power cycling – is associated with large junction temperature changes, ΔT_j

The die is connected to a low thermal impedance substrate, usually utilising copper in the form of so-called *direct copper bonding*, DCB, as shown in figure 5.8a and the forced water cooling effectiveness is shown in figure 5.7b.

Direct copper bonding
Direct copper bonding DCB is a process in which copper (on each side) and a ceramic material, usually either aluminium oxide (Al_2O_3) or aluminium nitride (AlN), are fused (bonded) together at high temperature.
The properties of DCB substrates are

- High mechanical strength and stability
- Good cohesion and corrosion resistance
- High electrical insulation
- Excellent thermal conductivity
- Reliable thermal cycling stability
- Matched thermal expansion coefficient to silicon and gallium arsenide
- Good heat spreading
- Processable, e.g. copper is etchable and millable like a pcb
- Environmentally friendly
- High copper current density

The advantages of DBC substrates are high current carrying capability due to thick copper metallization and a thermal expansion close to the silicon at the copper surface due to high bond strength of copper to ceramic. The DCB process yields a super-thin base and eliminates the need for the thick, heavy copper bases that were used prior to this process. Because power modules with DCB bases have fewer layers, they have a much lower thermal resistance. Because the expansion coefficient matches silicon, they have much better thermal cycling capabilities (up to 50,000 cycles). (See Appendix 5.13)

The drawback of standard DCB substrates for high voltage applications is a start of partial discharge at relatively low voltages. Therefore substrates using expensive metal brazing technologies (AMB) are mainly used in high voltage semiconductor modules for traction applications. The initiation voltage for a ceramic thickness of 0.63mm is less than 4kV. Main causes for this behaviour are small voids between the copper and ceramic and blurred straight border lines of the copper conductors at the copper/ceramic interface. Precision etching technology can alleviate these disadvantages. The other disadvantage of DCB is its deficiency for thermal shock because of the large residual stress on the substrate surface due to the coefficient of thermal expansion CTE mismatch of alumina and copper.

Thermal cycling

Intermittent equipment operation, start-up, and shutdown in extreme temperature conditions may cause power module thermal stresses due to the different linear expansion temperature co-efficients of the materials associated with the soldered substrate mounting to the copper base plate in multi-chip large area packages (see Tables 5.14 and 5.15 in Appendix 5.10). Large base plate (case) temperature changes in excess of 80K over a few minutes, stress the hard solder bonding between the copper base plate and the insulating substrate (usually AℓN or $A\ell_2 0_3$), as shown in figure 5.8a. This fatigue leads to eventual crack failure after a finite number of cycles *N*, as shown in figure 5.8c, approximated by

$$N = \frac{k}{A \times \Delta T^2} \tag{5.26}$$

where *A* is the die area and ΔT is the thermal shock temperature change. The constant *k* depends on the package, type of hard soldering, etc. Large, multiple die IGBT modules suffer from thermal shock limitations and relatively low reliability, because of the sheer large number of die soldered to the substrate over a large base plate copper area in the module.

Figure 5.8b shows how the number of thermal cycles to fracture for DCB substrates varies with copper thickness, when cycled between -40°C to +110°C. For a case temperature change of $\Delta T = 80$K, lifetime can be as low as 3,500 cycles and may only involve powering up and shutting down the associated equipment. Thermal cycling is normally performed by cycling the inactive package between the maximum and minimum storage temperatures. Although Aℓ/SiC is far superior to copper from a differential thermal expansion perspective, its thermal conductivity is only a little better than that of aluminium. Floating silicon wafers in disc type packages suffer to a much lesser extent (an order) from the effects of differential thermal expansion when thermally cycled. The use of a CuSiC base plate rather than copper can improve thermal cycling by a factor of ten.

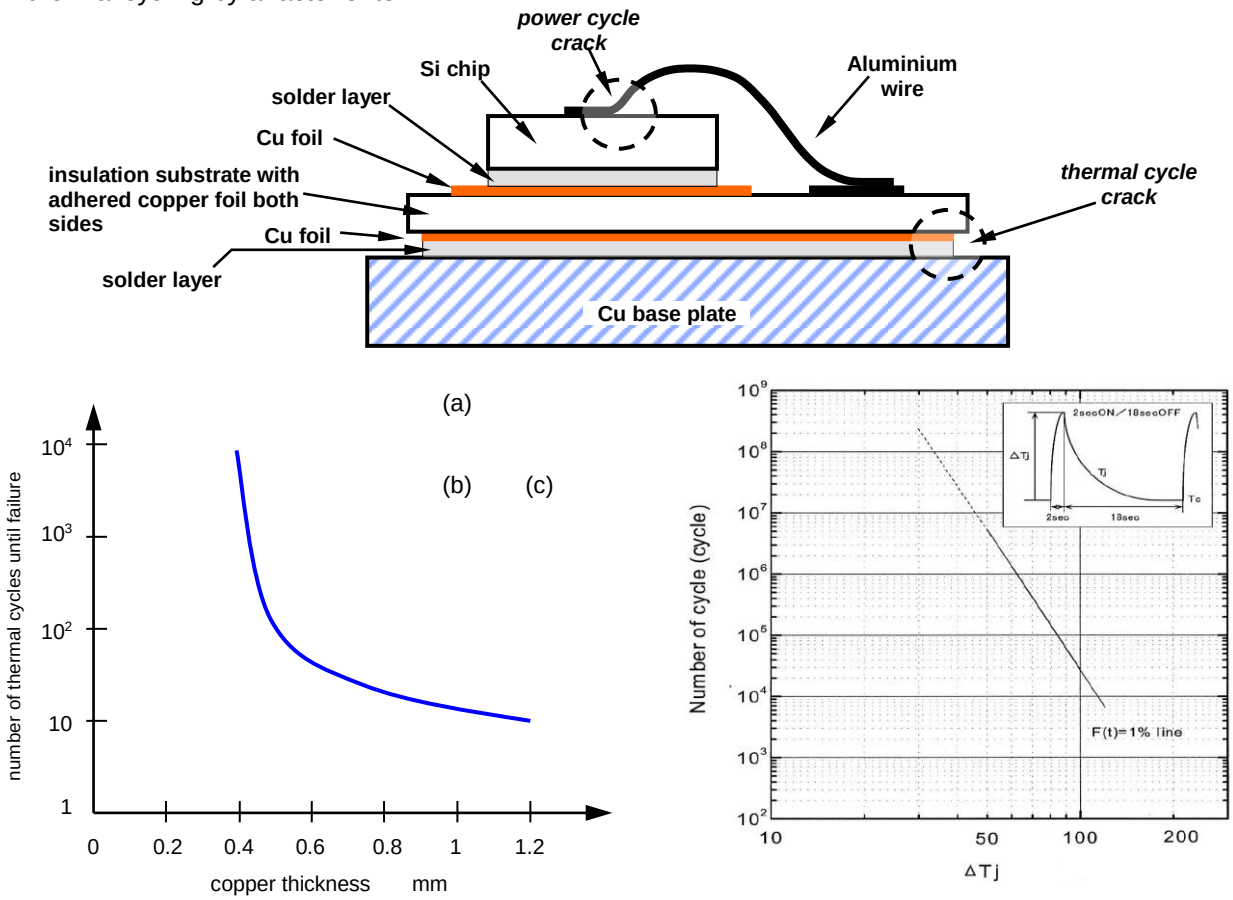

Figure 5.8. *Direct copper bonding:*
(a) sectional view of power module substrate showing boundary regions where power cycle cracking and thermal cycle cracking, occur; (b) copper thickness affect on power failure; and (c) power life thermal cycling.

Power cycling

Rapid cycling of the chip junction temperature causes mechanical stress around the silicon chip to aluminium wire bond interface, due to their different linear expansion temperature co-efficients. Eventually a crack occurs on the silicon side of the interface, as indicated in figure 5.8a. Short rapid junction temperature changes, over tens of seconds, of ΔT_j =100K, can lead to failure within 2500 cycles. The number of cycles to failure increases by just over an order for every 10°C decrease in ΔT_j.

In a related thermal application, where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. Figure 5.9 shows by comparison such a condition, where the operating frequency, not the maximum power dissipated, is dominant in determining junction temperature. In this case *thermal impedance* $Z_{\theta\,\text{j-c}}$ is used instead of thermal resistance $R_{\theta\,\text{j-c}}$ such that $Z_{\theta\,\text{j-c}} = r(t_p)\ R_{\theta\,\text{j-c}}$, where $r(t_p)$ is the normalising factor yielded from the normalised transient thermal impedance curves for the particular device. Appropriate values for the rectangular power pulse width t_p and duty cycle factor δ are used.

The power devices employed in power electronics are usually used in some form of on/off power pulse waveform mode. The following power waveforms are analysed:

- Periodic rectangular power pulses (steady-state thermal response);
- Single rectangular power pulse;
- Composite rectangular superimposed power pulses;
- A burst of rectangular power pulses; and
- Non-rectangular power pulses.

5.4.1 Steady-state response

Large cycle-by-cycle junction temperature fluctuations occur at low frequencies, figure 5.9a. As frequency increases, thermal inertia of the junction smoothes out instantaneous temperature fluctuations, as shown in figure 5.9b, and the junction responds more to average, rather than peak power dissipation. At frequencies above a kilohertz and duty cycles above 20 per cent, cycle-by-cycle temperature fluctuations usually become small, and the peak junction temperature rise approaches the average power dissipation multiplied by the steady-state junction-to-case thermal resistance, within a few per cent.

Because of thermal inertia (long thermal time constant), the heat sink and package case respond only to average power dissipation, except at ultra low frequencies, < 1Hz. The steady-state thermal conditions for the case-mount and junction (equation (5.12)) are given by

$$P_d = \frac{T_j - T_c}{R_{\theta j-c}} = \frac{T_c - T_a}{R_{\theta\text{c-s}} + R_{\theta\text{s-a}}} \quad \text{(W)} \qquad (5.27)$$

where P_d is the average power dissipation, which is the maximum power multiplied by the on-time duty cycle δ for rectangular power pulses. The difficulty in applying equation (5.27) often lies in determining the average power dissipation.

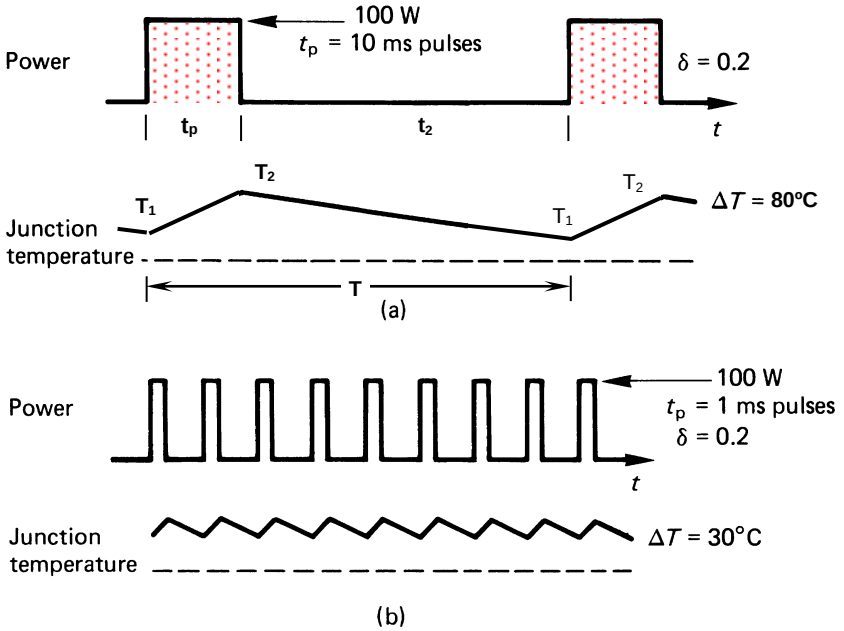

Figure 5.9. *Waveforms illustrating that peak junction temperature is a function of switching frequency: (a) lower switching frequency with 10 ms pulse and a 20 per cent duty cycle and (b) high frequency and 1 ms pulse with a duty cycle the same as in (a).*

5.4.2 Pulse response

When a junction dissipates power associated with a single pulse, the junction temperature increases during the pulse and decays to the original temperature after the energy pulse ceases. The junction temperature variation may vary from ambient temperature to a level above the normal maximum operating limit, a change of over 150°C. The upper temperature due to the power pulse can cause silicon damage, if the maximum allowable limit is exceeded too often or by a large amount on just a single occasion.

Equation (5.2) is valid for one dimensional steady state and transient thermal conditions, and the transient temperature equation is given by the first order solution to

$$P_d = -\frac{\lambda A}{\ell} T + \rho_m A \ell \frac{\delta T}{\delta t} \qquad \text{(W)} \tag{5.28}$$

The time domain solution for the temperature rise is

$$\Delta T(t) = \Delta \hat{T} \times \left(1 - e^{-t/\tau}\right) \tag{5.29}$$

where the maximum temperature eventually attained if the power pulse were maintained, above ambient, is

$$\Delta \hat{T} = \frac{P_d \ell}{\lambda A} = \frac{P_d}{h A} = P_d R_\theta \qquad (\text{K}) \tag{5.30}$$

and the thermal time constant

$$\tau = \frac{\rho_m \ell^2}{\lambda} = \frac{\text{thermal capacity, J/K}}{\text{power per K, W/K}} \qquad (\text{s}) \tag{5.31}$$

The transient thermal impedance Z_θ is defined as

$$Z_\theta = r(t_p) R_\theta = \frac{\Delta T}{P_d} = \frac{\Delta \hat{T} \times \left(1 - e^{-t_p/\tau}\right)}{\Delta T / R_\theta} = \left(1 - e^{-t_p/\tau}\right) R_\theta \tag{5.32}$$

That is, thermal resistance R_θ is modified by the factor $r(t_p)$ to yield transient thermal impedance Z_θ:

$$r(t_p) = \left(1 - e^{-t_p/\tau}\right) \tag{5.33}$$

This one-dimensional solution assumes a homogeneous thermal conducting material with a single point heat source, producing a uniform heat flow path. Since the practical case is far from ideal, manufacturers provide data for dynamic temperature effects based on the concept termed *thermal impedance*. The thermal solution given by equation (5.29) gives acceptable results when applied to solid carbon resistors (being a homogeneous material), as considered in Chapter 30 (specifically, see Example 30.7).

Example 5.1: ***Semiconductor single power pulse capability***

A semiconductor has a thermal capacity (*mc*) of 0.1J/K and a steady state thermal resistance to its case of R_θ = 0.5 K/W. If the junction temperature is not to exceed 125°C in a 25°C ambient, determine the allowable power dissipation, hence transient thermal impedance, as a function of single power pulse duration. Plot the results for five time decades, decreasing from 1s.

Solution

The power dissipation per K is

$$P_d / \text{K} = \frac{1}{R_\theta} = \frac{1}{0.5\,\text{K/W}} = 2\,\text{W/K}$$

From equation (5.31) the thermal time constant τ is given by

$$\tau = \frac{\text{thermal capacity, J/K}}{\text{power per K, W/K}} = \frac{0.1\,\text{J/K}}{2\,\text{W/K}} = 0.05\text{s}$$

After time t_p, the junction temperature rise from 25°C must not exceed 125°C, that is $\Delta T(t_p) = 100$K, thus equation (5.29) gives

$$\Delta T(t_p) = \Delta \hat{T} \times \left(1 - e^{-t/\tau}\right) = \Delta \hat{T} \times \left(1 - e^{-t_p/0.05\text{s}}\right) = 100\text{K}$$

As a specific example of the procedure, consider a t_p = 10ms energy pulse.

$$\Delta T(10\text{ms}) = \Delta \hat{T} \times \left(1 - e^{-10\text{ms}/0.05\text{s}}\right) = 100\text{K}$$

which yields $\Delta\hat{T} = 551.6\text{K}$. That is, after a long period (>>10ms) the junction temperature would increase by 551.6K. From equation (5.30), this temperature rise corresponds to continuous power of

$$P_d = \frac{\Delta\hat{T}}{R_\theta} = \frac{551.6\text{K}}{0.5\text{K/W}} = 1103.3\text{W}$$

In 10ms the temperature must only rise 100K, hence, from equation (5.32) the transient thermal impedance Z_θ is

$$Z_\theta = r\left(t_p\right)R_\theta = \frac{\Delta T}{P_d} = \frac{100\text{K}}{1103.3\text{W}} = 0.091\text{K/W}$$

Thus the thermal resistance R_θ is modified, or normalized, by

$$r\left(10\text{ms}\right) = \frac{Z_\theta}{R_\theta} = \frac{0.0001\text{K/W}}{0.5\text{K/W}} = 0.181$$

Table 5.7 shows the normalised thermal impedance factor, $r(t_p)$, for other pulse durations, which are plotted in the accompanying figure. Notice the similarity of the single pulse results given for a practical power device in figure 5.10.

Table 5.7: Single pulse data

t_p	$\Delta\hat{T}$ $t \to \infty$	P_d $= \Delta\hat{T}/R_\theta$	Z_θ $= \Delta T/P_d$	$r\,(t_p)$ $= Z_\theta\ /R_\theta$
pulse time	temperature rise	power dissipated	thermal impedance	normalised
s	K	W	K/W	pu
1	100	200	0.5	1
0.1	116	231	0.432	0.86
0.01	552	1103	0.091	0.181
0.001	5050	10100	0.0099	0.0198
0.0001	50050	100100	0.0010	0.0020
0.00001	500050	1000100	0.0001	0.0002

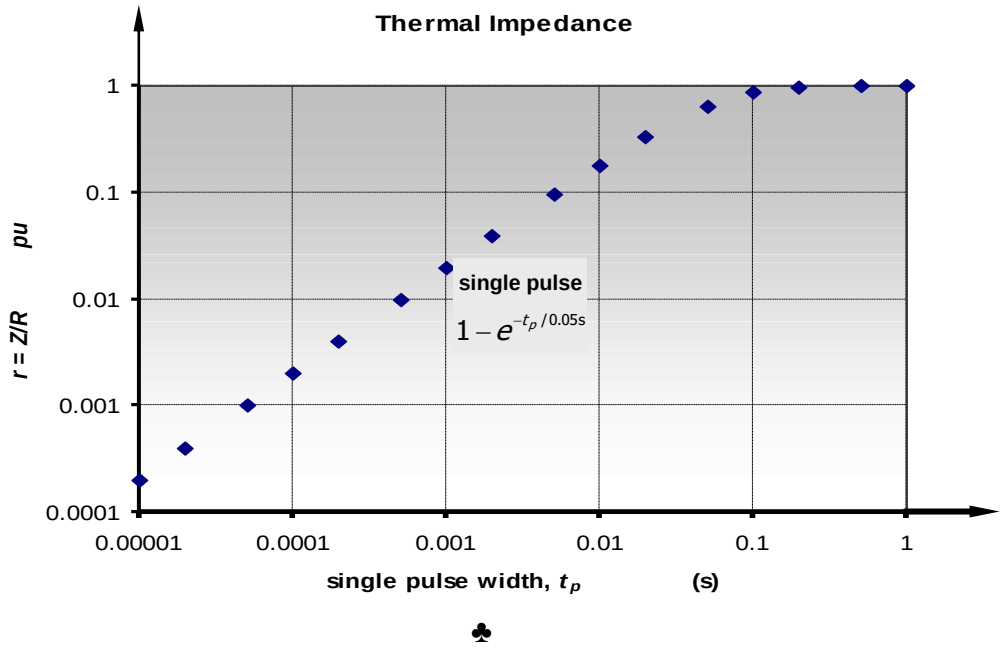

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Figure 5.10 shows the thermal impedance curves for a power-switching device, normalised with respect to the steady-state thermal resistance $R_{\theta\,\text{j-c}}$. The curve labelled 'single pulse' shows the rise of junction temperature per watt of power dissipated as a function of pulse duration. The thermal impedance for repetitive pulses Z, of duty cycle δ, can be determined from the single pulse value z according to

$$Z_\theta\left(t_p, \delta\right) = \delta + \left(1-\delta\right)z\left(t_p\right) \qquad \text{(K/W)} \qquad (5.34)$$

Equation (5.12) becomes

$$P_p = \frac{\hat{T}_j - T_c}{Z_\theta(t_p, \delta)} = \frac{\hat{T}_j - T_c}{r(t_p)R_{\theta j-c}} \quad \text{(W)} \qquad (5.35)$$

Note that the peak power P_p is employed, and then only for thermal analysis from the junction to the case thermal mounting. That is, $Z_{\theta j\text{-}c}$ is the only thermal impedance term that exists. See problem 5.8.

Figure 5.10 shows that at the pulse width minimum extreme, $t_p < 1\mu s$, as $z(t_p \to 0) \to 1$ in equation (5.34):

$$\lim_{t_p \to 0} Z_\theta(0, \delta) = \delta R_{\theta j-c} = r(t_p = 0) R_{\theta j-c} \qquad (5.36)$$

that is, $r(t_p \to 0) \to \delta$.

Figure 5.10 also shows that at the pulse maximum extreme, that is, $t_p > 1s$ or continuous power dissipation, as $z(t_p \to 1) \to 0$ in equation (5.34):

$$\lim_{t_p \to \infty} Z_\theta(\infty, \delta) = R_{\theta j-c} \qquad (5.37)$$

that is, $r(t_p \to \infty) \to 1$, independent of duty cycle, that is, for all duty cycles.

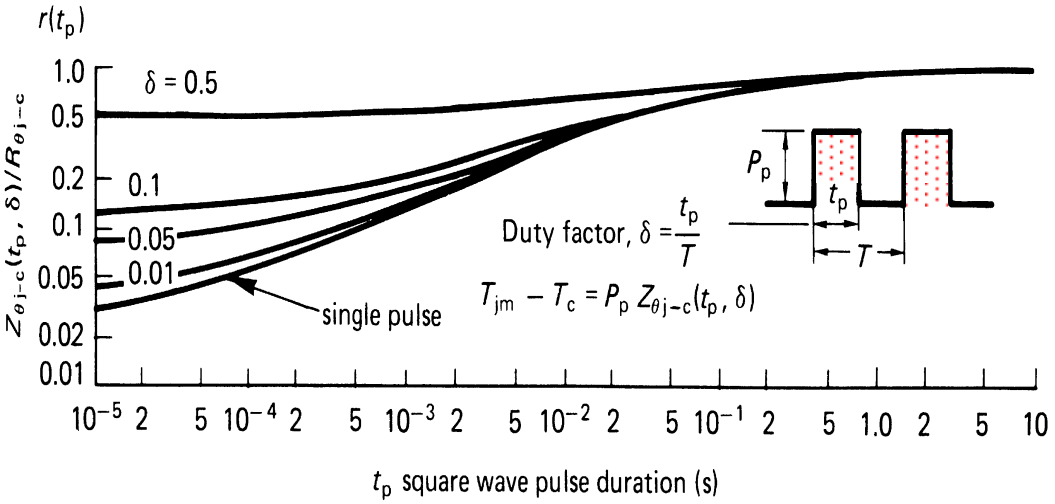

Figure 5.10. *Transient thermal impedance curves; normalised with respect to the steady state thermal resistance,* $R_{\theta\,j\text{-}c}$.

Example 5.2: ***A single rectangular power pulse***

A semiconductor with a junction to case thermal resistance of 1 K/W absorbs a single 100W power pulse for 20μs. Based on the thermal impedance characteristics in figure 5.10, what is the expected junction temperature rise, assuming the case-mount temperature does not respond to this short pulse?

Solution

The period for a single power pulse is infinite $T \to \infty$, therefore the duty cycle t_p / T is zero, $\delta = 0$.

$$\Delta T_{j-c} = P \times Z_{\theta j-c} = P \times r(t_p) \times R_{\theta j-c}$$

From figure 5.10, for a single 20μs pulse $r(t_p = 20\mu s) = 0.035$. The junction temperature change is therefore

$$\Delta T_{j-c} = P \times r(t_p = 20\mu s) \times R_{\theta j-c}$$
$$= 100\text{W} \times 0.035 \times 1\text{K/W} = 3.5\text{K}$$

The peak junction temperature will rise to 3.5K above the case mount temperature at the end of the 100W rectangular power pulse.

♣

The basic single rectangular power pulse approach can be extended to analyse composite rectangular power pulses by algebraic superposition of a series of accumulating rectangular pulses. Because each composite power pulse extends to the end of the temperature-calculating period, any positive rectangular pulse is subsequently cancelled by a negative power pulse. The technique is illustrated in example 5.4.

5.4.3 Repetitive transient response

Minimal temperature variation occurs if the power switching period T is shorter than the junction to case mount thermal time constant, $T < \tau$, whence the concept of steady state thermal resistance is applicable, as presented in 5.4.1. When the relative magnitudes are reversed such that $T > 5\,\tau$, then the temperature effects of the power pulse die away, and the single pulse transient thermal impedance approach presented in 5.4.2 is applicable.

The transition or boundary between junction operation that can be assumed steady-state junction temperature operation ($T < \tau$) and that of a series of discrete non-interacting single pulses ($T > 5\,\tau$) can be analysed by extending the one-dimensional thermal transient equation (5.29) in conjunction with figure 5.9a. Figure 5.9a shows how the temperature increases from T_1 to T_2 during the time t_p when power is dissipated, and decreases from T_2 to T_1 during time t_2 when no power is being dissipated by the virtual junction. This increasing and decreasing of the junction temperature occurs cyclically over each period T. Based on equation (5.29) the junction temperature increases exponentially according to

$$T(t) = \Delta\hat{T} - \left(\Delta\hat{T} - T_1\right)e^{-t/\tau} \tag{5.38}$$

and decreases exponentially according to

$$T(t) = T_2\, e^{-t/\tau} \tag{5.39}$$

where the thermal time constant τ and maximum possible junction temperature rise are defined by equations (5.31) and (5.30), respectively. Since these temperature variations are in steady state, the temperature constants T_1 to T_2 can be solve using the boundary conditions. This gives

$$T_2 = \Delta\hat{T}\,\frac{1 - e^{-t_p/\tau}}{1 + e^{-T/\tau}} \quad \text{and} \quad T_1 = T_2\, e^{-t_2/\tau} \tag{5.40}$$

The junction temperature swing, ΔT is

$$\Delta T_j = T_2 - T_1 = \Delta\hat{T}\,\frac{\left(1 - e^{-t_p/\tau}\right)\left(1 - e^{-t_2/\tau}\right)}{1 + e^{-T/\tau}} \tag{5.41}$$

The maximum variation in junction temperature occurs for square-wave power, that is $t_p = t_2 = ½T$, $\delta = ½$:

$$\Delta T_j^{\max} = \Delta\hat{T}\tanh\left(\frac{T}{4\tau}\right) \tag{5.42}$$

This equation highlights that the magnitude of the temperature change is highly dependant on the power switching frequency $1/T$ relative to the thermal time constant τ of the semiconductor package.

Example 5.3: ***Semiconductor transient repetitive power capability***

A semiconductor with a thermal capacity of 0.02J/K and a thermal resistance from the junction to the case of ½K/W, dissipates 100W at a repetition rate of

i. 50Hz
ii. 300Hz.

By calculating the worst-case junction temperature variation, indicate whether steady-state constant junction temperature-based analysis (a thermal resistance approach) is a valid assumption.

Solution

The long-term junction temperature rise with 100W continuous is given by equation (5.30), which yields

$$\Delta\hat{T} = P_d\, R_\theta = 100\text{W} \times ½\text{K/W} = 50\text{K}$$

The thermal time constant τ is given by equation (5.31), giving

$$\tau = \frac{\text{thermal capacity, J/K}}{\text{power per K, W/K}} = \frac{0.02}{1/½} = 0.01 \quad (\text{s})$$

Worst case temperature variation occurs with a 50% power duty cycle, as given by equation (5.42)

$$\Delta T_j^{\max} = \Delta\hat{T}\tanh\left(\frac{T}{4\tau}\right) = 50\text{K} \times \tanh\left(\frac{T}{4 \times 0.01\text{s}}\right)$$

From this equation:

at 50Hz, $T = 20\text{ms}$, $\Delta T_j^{\max} = 23.1\text{K}$

at 300Hz, $T = 3.33\text{ms}$, $\Delta T_j^{\max} = 4.1\text{K}$

The temperature variation of 4.1K at 300Hz is small compared to the maximum allowable junction temperature, typical between 125°C and 175ºC, thus thermal analysis of this device in a 300Hz

application, can be thermal resistance calculation based as presented in 5.4.1. On the other hand, the same device used in a 50Hz application will experience 5.6 times the junction temperature swing. This 23.1K variation represents a significant portion of the allowable junction operating temperature, and could mean a thermal resistance approach is unsafe. A thermal impedance design approach is recommended, as in example 5.2 and 5.4.2.

♣

Example 5.4: ***Composite rectangular power pulses***

A semiconductor with a junction to case thermal resistance of 1 K/W absorbs the composite power pulse shown in figure 5.11. Based on the thermal impedance characteristics in figure 5.12, what is the expected junction temperature rise at indicate times t_x and t_y, assuming the case temperature does not respond to this short pulse? That is, the heatsink-case interface temperature is held constant.
What is the average junction to case temperature rise, in the repetitive case, f=2kHz?

Solution

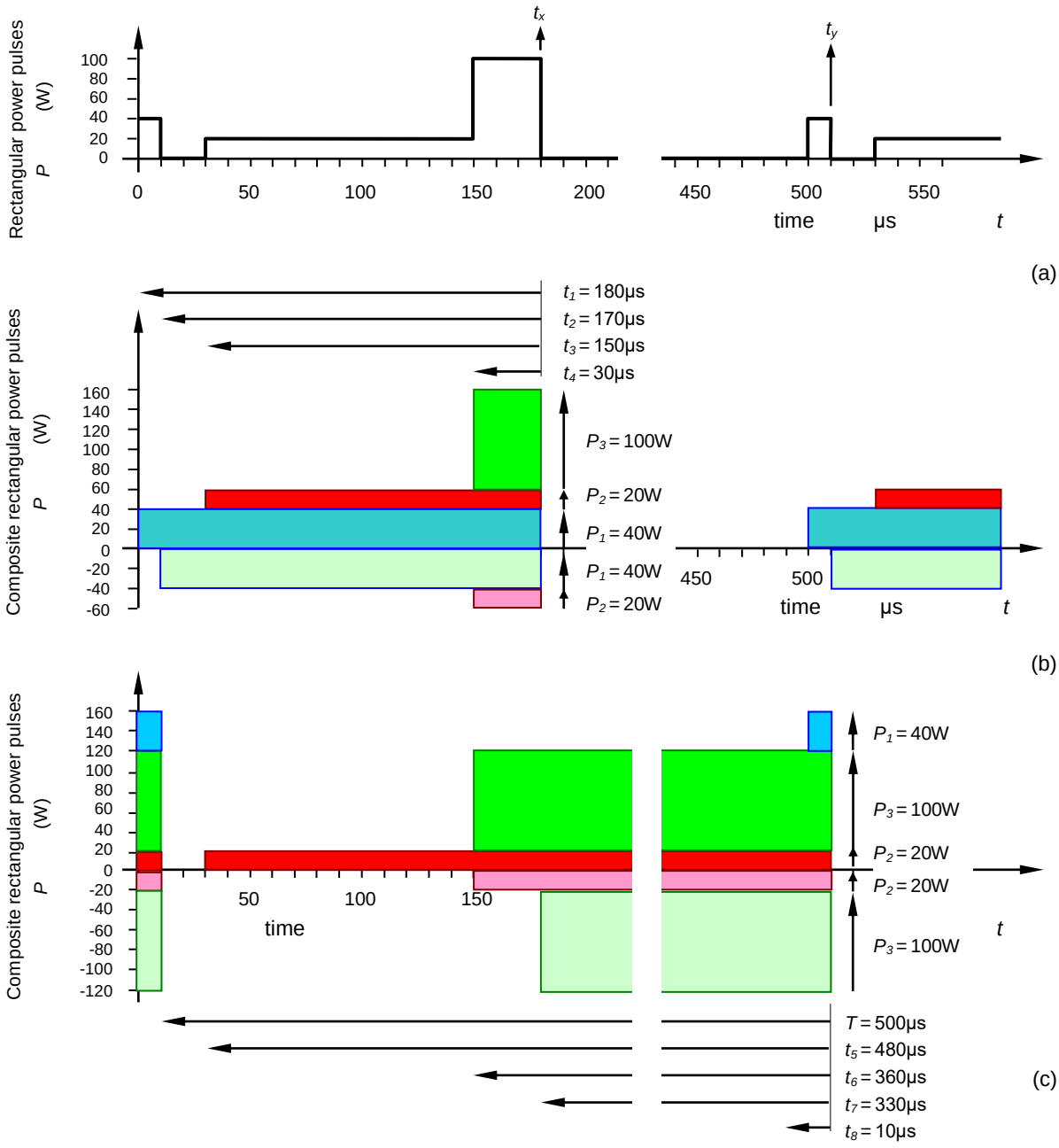

Figure 5.11. *Composite power pulses: (a) original rectangular pulse; (b) composite rectangular pulse, reference t_x; and (c) composite rectangular pulse, reference t_y.*

Table 5.8: Rectangular, composite pulse example data

		t_x				t_y			
Pulse duration		t_{p1}	t_{p2}	t_{p3}	t_{p4}	t_{p5}	t_{p6}	t_{p7}	t_{p8}
		180µs	170µs	150µs	30µs	480µs	360µs	330µs	10µs
single pulse	$\delta = t_p / T$	0	0	0	0	0	0	0	0
$T \rightarrow \infty$	$r(t_p)$	0.06	0.055	0.05	0.025	0.10	0.085	0.08	0.015
period	$\delta = t_p / T$	0.36	0.34	0.30	0.06	0.96	0.72	0.66	0.02
$T = 500$µs	$r(t_p)$	0.38	0.36	0.35	0.075	0.96	0.73	0.73	0.035

In figure 5.11b, power pulse $P_1 = 40$W lasts for 180µs, which represents a duty cycle of δ=180µs/500µs = 0.36. The thermal impedance normalised factor of $r(t_{p1}$=80µs) = 0.38 corresponds to $\delta = 0.45$ in figure 5.12.

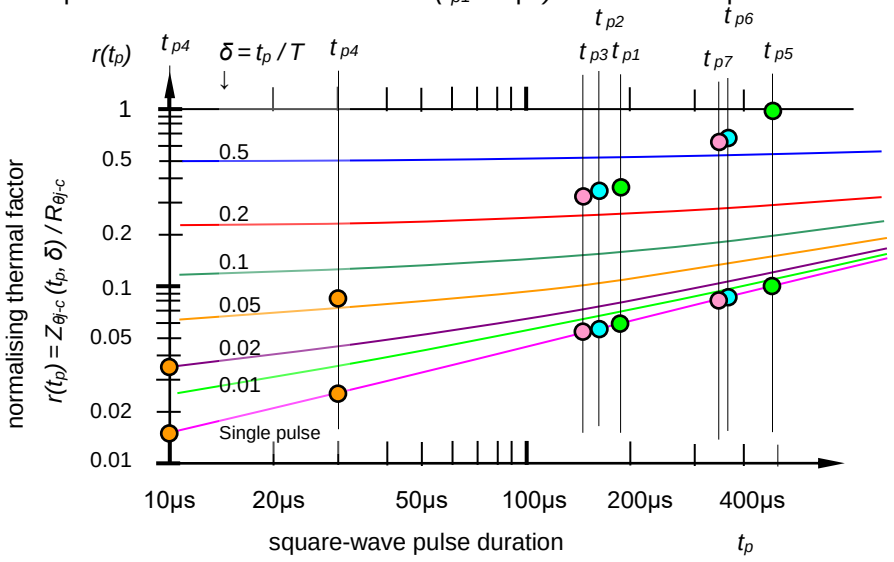

Figure 5.12. *Normalise junction to case-mount thermal impedance characteristics.*

The junction temperature (rise) at t_x, is given by

$$T_{j-c}^{t_x} = P_1 Z_{\theta j-c}^{tp1} - P_1 Z_{\theta j-c}^{tp2} + P_2 Z_{\theta j-c}^{tp3} - P_2 Z_{\theta j-c}^{tp4} + P_3 Z_{\theta j-c}^{tp4}$$

The junction temperature (rise) at t_y, is given by

$$T_{j-c}^{t_y} = P_2 Z_{\theta j-c}^{tp5} - P_2 Z_{\theta j-c}^{tp6} + P_3 Z_{\theta j-c}^{tp6} - P_3 Z_{\theta j-c}^{tp7} + P_1 Z_{\theta j-c}^{tp8}$$

t_x repetitive

$$\begin{aligned} T_{j-c}^{t_x} &= 40 \times Z_{\theta j-c}^{tp1} - 40 \times Z_{\theta j-c}^{tp2} + 20 \times Z_{\theta j-c}^{tp3} - 20 \times Z_{\theta j-c}^{tp4} + 100 \times Z_{\theta j-c}^{tp4} \\ &= 40 \times 0.38 \times 1\text{K/W} - 40 \times 0.36 \times 1\text{K/W} + 20 \times 0.35 \times 1\text{K/W} - 20 \times 0.075 \times 1\text{K/W} + 100 \times 0.075 \times 1\text{K/W} \\ &= 13.8\text{K} \end{aligned}$$

t_x single pulse

$$\begin{aligned} T_{j-c}^{t_x} &= 40 \times Z_{\theta j-c}^{tp1} - 40 \times Z_{\theta j-c}^{tp2} + 20 \times Z_{\theta j-c}^{tp3} - 20 \times Z_{\theta j-c}^{tp4} + 100 \times Z_{\theta j-c}^{tp4} \\ &= 40 \times 0.06 \times 1\text{K/W} - 40 \times 0.055 \times 1\text{K/W} + 20 \times 0.05 \times 1\text{K/W} - 20 \times 0.025 \times 1\text{K/W} + 100 \times 0.025 \times 1\text{K/W} \\ &= 2.7\text{K} \end{aligned}$$

t_y repetitive

$$\begin{aligned} T_{j-c}^{t_y} &= 20 \times Z_{\theta j-c}^{tp5} - 20 \times Z_{\theta j-c}^{tp6} + 100 \times Z_{\theta j-c}^{tp6} - 100 \times Z_{\theta j-c}^{tp7} + 100 \times Z_{\theta j-c}^{tp8} \\ &= 20 \times 0.96 \times 1\text{K/W} - 20 \times 0.73 \times 1\text{K/W} + 100 \times 0.73 \times 1\text{K/W} - 100 \times 0.67 \times 1\text{K/W} + 40 \times 0.035 \times 1\text{K/W} \\ &= 12.2\text{K} \end{aligned}$$

t_y single pulse

$$T_{j-c}^{t_y} = 20 \times Z_{\theta j-c}^{tp5} - 20 \times Z_{\theta j-c}^{tp6} + 100 \times Z_{\theta j-c}^{tp6} - 100 \times Z_{\theta j-c}^{tp7} + 100 \times Z_{\theta j-c}^{tp8}$$
$$= 20 \times 0.10 \times 1\text{K/W} - 20 \times 0.085 \times 1\text{K/W} + 100 \times 0.085 \times 1\text{K/W} - 100 \times 0.08 \times 1\text{K/W} + 40 \times 0.015 \times 1\text{K/W}$$
$$= 1.4\text{K}$$

In the repetitive composite pulse case, the average power dissipated over 500μs is

$$\frac{10\mu\text{s} \times 40\text{W} + 120\mu\text{s} \times 20\text{W} + 30\mu\text{s} \times 100\text{W}}{500\mu\text{s}} = 11.6\text{W}$$

The average junction to case mounting temperature rise is

$$T_{j-c} = P_{ave} \times R_{\theta j-c} = 11.6\text{W} \times 1\text{K/W} = 11.6\text{K}$$

♣

Non-rectangular power pulses

The concept and characterisation of thermal impedance is based on rectangular power pulses. Non-rectangular pulses are converted to equivalent energy, rectangular pulses having the same peak power, P_p, of duration t_p, as shown in figure 5.13. The resultant rectangular power pulse will raise the junction temperature higher than any other wave shape with the same peak and average values, since it concentrates its heating effects into a shorter period of time, thus minimising cooling during the pulse. Worst case semiconductor thermal conditions result. Improved thermal accuracy is obtained if each non-rectangular pulse is further sub-divided into numerous equivalent total energy rectangular pulses, as considered in example 5.5.

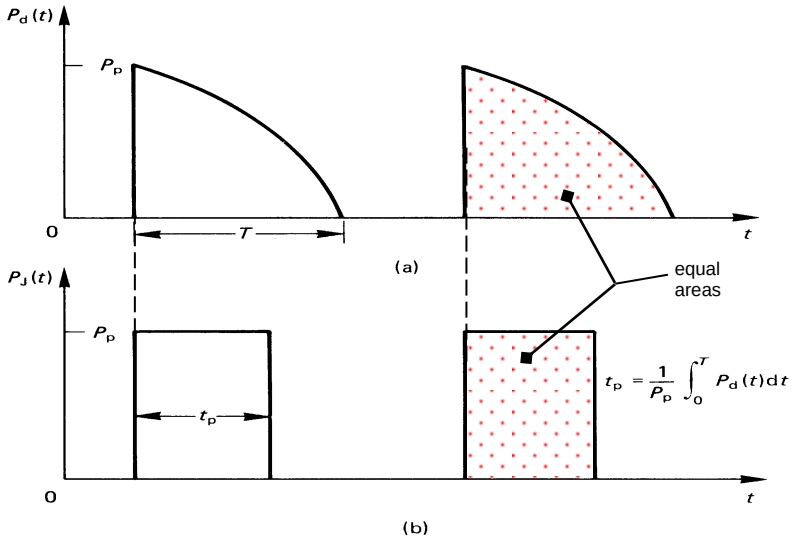

Figure 5.13. *Conversion of non-rectangular power pulse (a) into equivalent rectangular pulse (b).*

Example 5.5: ***Non-rectangular power pulses***

Switch losses are a series of triangular power pulses rising linearly to 100W in 100μs after switch turn-on. If the thermal resistance of the junction to case mounting is 1 K/W and the thermal impedance characteristics are represented by figure 5.15, calculate the case to junction peak temperature rise for

i. A single pulse, $T \rightarrow \infty$
ii. 50% power duty cycle, $T = 200\mu\text{s}$
iii. 10% duty cycle, $T = 1000\mu\text{s}$

Represent the triangular power pulses by firstly one equivalent rectangular power pulse, secondly two equivalent rectangular power pulses, and compare the predicted peak junction temperature rise results. Assume the case temperature is maintained at a constant temperature.
Where applicable, calculate the average junction to case thermal mounting temperature drop, $T_{j\text{-}c}$.

Solution

Each saw-tooth power pulse is represented by a single rectangular power pulse, 100W and 50μs duration in figure 5.14, therein fulfilling the requirements of the same maximum power occurring simultaneously in both waveforms and both containing the same energy, area.

Figure 5.14 also shows the two rectangular pulse representations, where successive 50μs portions of the triangle are represent by pulses, 100W, 37.5μs and 50W, 25μs, such that the total area is maintained and the peak junction temperature rise occurs at the end of the power pulse sequence. The two pulses are subsequently decomposed into three equivalent composite rectangular power pulses, which sum at any time to give the original two rectangular pulses.

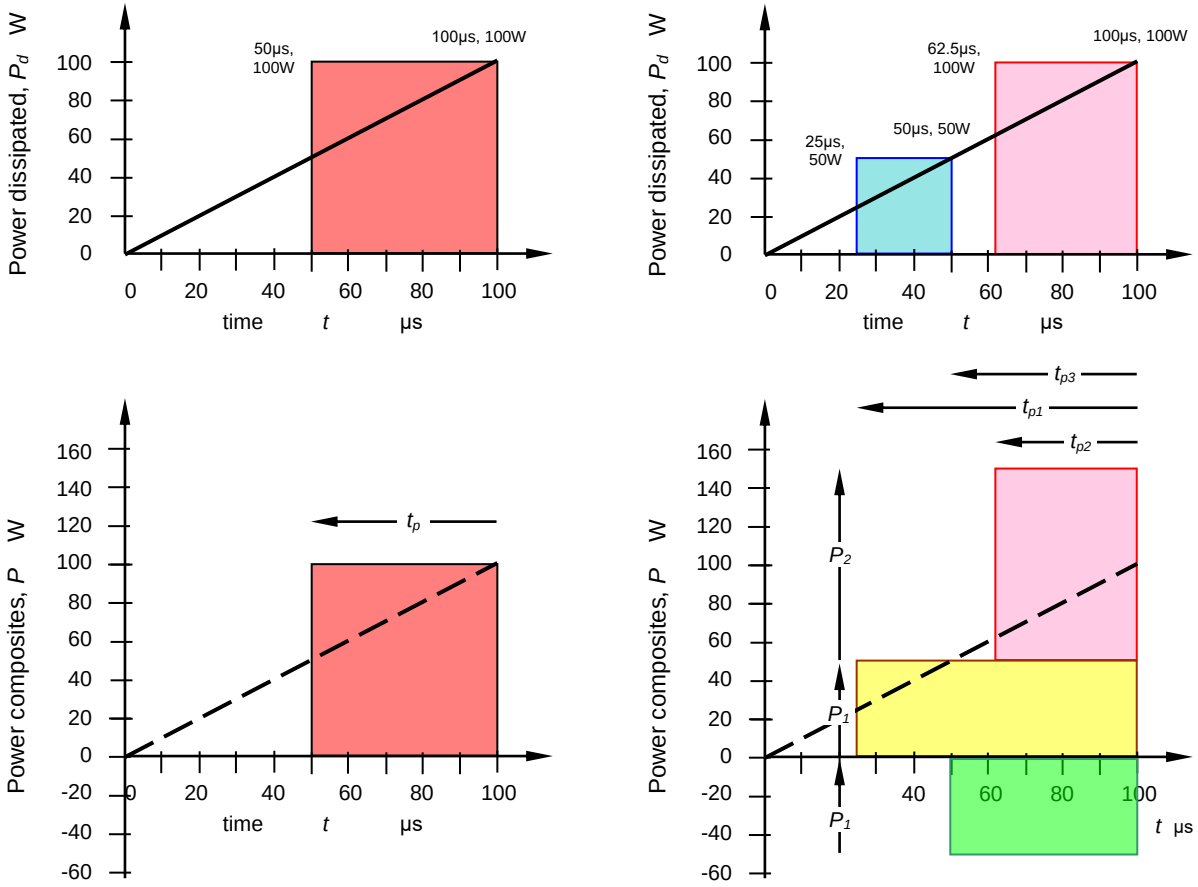

Figure 5.14. *Transient thermal impedance curves; normalised with respect to the steady state thermal resistance,* $R_{\theta\,j\text{-}c}$.

The thermal impedance normalising factor $r(t_p)$ for the applicable device can be read from figure 5.15, using the pulse periods and duty cycles shown in figure 5.14, and are shown in Table 5.9.

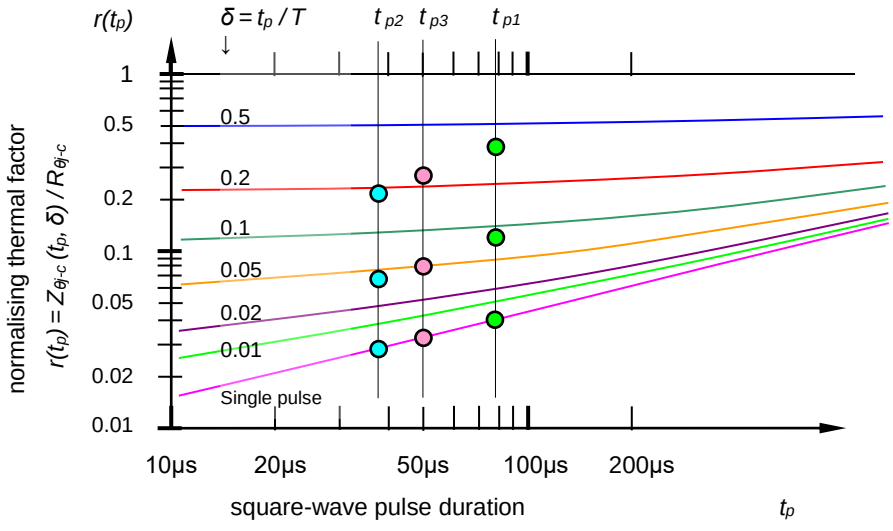

Figure 5.15. *Transient thermal impedance curves; normalised with respect to the steady state thermal resistance,* $R_{\theta\,j\text{-}c}$.

Table 5.9: Non-rectangular, composite pulse example data

		One composite power pulse	Two composite power pulses		
Pulse duration		t_p	t_{p1}	t_{p2}	t_{p3}
		50μs	75μs	37.5μs	50μs
Single pulse $T \to \infty$	$\delta = t_p / T$	0	0	0	0
	$r(t_p)$	0.045	0.04	0.040	0.045
50% duty cycle $T = 200\mu s$	$\delta = t_p / T$	¼	⅜	0.188	¼
	$r(t_p)$	0.32	0.40	0.22	0.32
10% duty cycle $T = 1000\mu s$	$\delta = t_p / T$	0.05	0.075	0.0375	0.05
	$r(t_p)$	0.08	0.12	0.066	0.08

For a single pulse rectangular power waveform

$$\begin{aligned}\Delta T_{j-c} &= P \times Z_{\theta j-c} = P \times r\left(t_p\right) \times R_{\theta j-c} \\ &= 100\text{W} \times r\left(t_p = 50\mu\text{s}\right) \times 1\text{K/W}\end{aligned}$$

For a single pulse, $\delta = 0$

$$\begin{aligned}\Delta T_{j-c} &= 100\text{W} \times r\left(t_p = 50\mu\text{s}\right) \times 1\text{K/W} \\ &= 100\text{W} \times 0.045 \times 1\text{K/W} = 4.5\text{K}\end{aligned}$$

For a 50% duty cycle, $\delta = 0.5$

$$\begin{aligned}\Delta T_{j-c} &= 100\text{W} \times r\left(t_p = 50\mu\text{s}\right) \times 1\text{K/W} \\ &= 100\text{W} \times 0.32 \times 1\text{K/W} = 32\text{K}\end{aligned}$$

For a 10% duty cycle, $\delta = 0.1$

$$\begin{aligned}\Delta T_{j-c} &= 100\text{W} \times r\left(t_p = 50\mu\text{s}\right) \times 1\text{K/W} \\ &= 100\text{W} \times 0.08 \times 1\text{K/W} = 8\text{K}\end{aligned}$$

For a two pulse rectangular power waveform representation

$$\begin{aligned}\Delta T_{j-c} &= P_1 \times Z_{\theta j-c\ t1} - P_1 \times Z_{\theta j-c\ t3} + P_2 \times Z_{\theta j-c\ t2} \\ &= P_1 \times r\left(t_{p1}\right) \times R_{\theta j-c\ t1} - P_1 \times r\left(t_{p3}\right) \times R_{\theta j-c\ t3} + P_2 \times r\left(t_{p2}\right) \times Z_{\theta j-c\ t2} \\ &= 50\text{W} \times r\left(t_{p1} = 75\mu\text{s}\right) \times 1\text{K/W} - 50\text{W} \times r\left(t_{p3} = 50\mu\text{s}\right) \times 1\text{K/W} + 100\text{W} \times r\left(t_{p2} = 37.5\mu\text{s}\right) \times 1\text{K/W}\end{aligned}$$

For a single pulse, $\delta = 0$

$$\begin{aligned}\Delta T_{j-c} &= 50\text{W} \times r\left(t_{p1} = 75\mu\text{s}\right) \times 1\text{K/W} - 50\text{W} \times r\left(t_{p3} = 50\mu\text{s}\right) \times 1\text{K/W} + 100\text{W} \times r\left(t_{p2} = 37.5\mu\text{s}\right) \times 1\text{K/W} \\ &= 50\text{W} \times 0.04 \times 1\text{K/W} - 50\text{W} \times 0.045 \times 1\text{K/W} + 100\text{W} \times 0.04 \times 1\text{K/W} \\ &= 3.75\text{K}\end{aligned}$$

For a 50% duty cycle, $\delta = 0.5$

$$\begin{aligned}\Delta T_{j-c} &= 50\text{W} \times r\left(t_{p1} = 75\mu\text{s}\right) \times 1\text{K/W} - 50\text{W} \times r\left(t_{p3} = 50\mu\text{s}\right) \times 1\text{K/W} + 100\text{W} \times r\left(t_{p2} = 37.5\mu\text{s}\right) \times 1\text{K/W} \\ &= 50\text{W} \times 0.40 \times 1\text{K/W} - 50\text{W} \times 0.32 \times 1\text{K/W} + 100\text{W} \times 0.22 \times 1\text{K/W} \\ &= 26\text{K}\end{aligned}$$

For a 10% duty cycle, $\delta = 0.1$

$$\begin{aligned}\Delta T_{j-c} &= 50\text{W} \times r\left(t_{p1} = 75\mu\text{s}\right) \times 1\text{K/W} - 50\text{W} \times r\left(t_{p3} = 50\mu\text{s}\right) \times 1\text{K/W} + 100\text{W} \times r\left(t_{p2} = 37.5\mu\text{s}\right) \times 1\text{K/W} \\ &= 50\text{W} \times 0.12 \times 1\text{K/W} - 50\text{W} \times 0.08 \times 1\text{K/W} + 100\text{W} \times 0.066 \times 1\text{K/W} \\ &= 8.6\text{K}\end{aligned}$$

The average junction to case temperature for a single pulse is zero, and the average junction temperature is the heatsink/ambient temperature.

The average junction to case temperature during repetitive operation is independent of whether one or two composite rectangular pulses are used to analyse the saw-tooth pulse pulses, since both model the same original power waveform, each having the same waveform area, energy. The junction to case temperature is dependent on the duty cycle, which specifies the average power dissipation.

$$\overline{P}_d = \frac{\text{sawtooth area}}{T}$$
$$= \frac{½ \times 100\text{W} \times 100\mu\text{s}}{T} = \delta \times 50\,\text{W}$$

Thus the average case to junction temperature drop is

$$T_{j-c} = \overline{P}_d \times R_{\theta j-c}$$
$$= \delta \times 50\text{W} \times 1\text{K/W} = 50 \times \delta\,\text{K}$$

For 50% and 10% duty cycles, this gives average temperature drops of 25K and 5K respectively.

Both rectangular composite power pulse decomposition assumptions produce similar thermal results. At cycle frequencies of 5kHz and 1kHz, together with high duty cycles, the peak junction temperature is marginally higher than the average junction temperature. Using the concept of thermal resistance is adequate under the switching frequency and duty cycle conditions of this problem.

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5.5 Average power dissipation

Two commonly used empirical methods for determining power dissipation P_d are

- graphical integration and
- power superposition.

5.5.1 Graphical integration

Graphical integration may be formulated by digitally storing a complete cycle of test device voltage and current under limiting steady-state temperature conditions. Each voltage and current time-corresponding pair are multiplied together to give instantaneous values of power loss. Numerical integration techniques are then employed to give the average power dissipation.

5.5.2 Practical superposition

This technique is based on substituting a smooth dc voltage source for a complex waveform. A two-pole, two-position switching arrangement is used, which firstly allows operation of the load with the device under test, until the monitored case temperature stabilises. Then, by throwing the switch to the test mode position, the device under test (DUT) is connected to a dc power supply, while the other pole of the switch supplies the normal power to the load to keep it operating at full power level conditions. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc source voltage and current values are multiplied together to obtain the average power dissipated.

5.6 Power losses from manufacturers' data sheets

The total power dissipation P_d is the sum of the switching transition loss P_s, the on-conduction loss P_d, drive input device loss P_G, and the off-state leakage loss P_ℓ.
The average total power loss is given by

$$P_d = f_s \int_0^{1/f_s} v(t)\, i(t)\, dt \qquad \text{(W)} \qquad (5.43)$$

where f_s is the switching frequency and $v(t)$ and $i(t)$ are the device instantaneous voltage and current over one complete cycle of period $1/f_s$. The usual technique for determining total power loss is to evaluate and sum together each of the individual average power loss components.

5.6.1 Switching transition power loss, P_s

Figure 5.16 shows typical power device voltage-current switching waveforms. Normally an exact solution is not required and an approximation based on straight-line switching intervals is usually adequate.
For a resistive load, as derived in Chapter 7

$$P_s = \tfrac{1}{6} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.44)$$

and for an inductive load, as derived in Chapter 7

$$P_s = ½ V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.45)$$

where τ is the period of the switching interval (both on and off), and V_s and I_m are the maximum voltage and current levels as shown in figure 5.16. Switching losses occur at both turn-on and turn-off.

5.6.2 Off-state leakage power loss, P_ℓ

During the switched-off period, a small, exponentially temperature dependent current I_ℓ, will flow through the switch. The loss due to this leakage current is

$$P_\ell = I_\ell V_s (1-\delta) \quad \text{(W)} \tag{5.46}$$

where δ is the on-time duty cycle of the switch. Normally P_ℓ is only a small part of the total loss so that the error in neglecting P_ℓ is not significant.

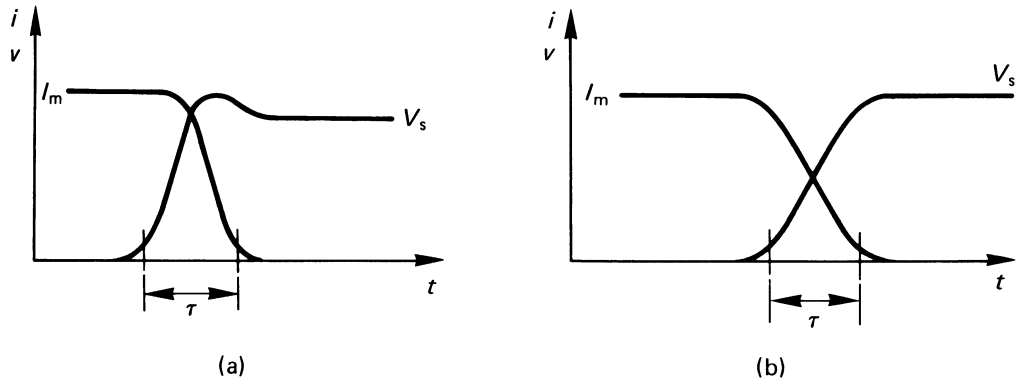


Figure 5.16. *Typical voltage and current at turn-off switching transition for: (a) an inductive load and (b) a resistive load. Current and voltage are interchanged at turn-on.*

5.6.3 Conduction power loss, P_c

The average conduction power loss under a steady-state current condition is given by

$$P_c = \delta I_{on} V_{on} \quad \text{(W)} \tag{5.47}$$

although equation (5.43) is valid in the general case when the integration is performed over the interval corresponding to δ.

The conduction loss for the MOSFET is usually expressed in terms of its on-state resistance (equations (3.16) and (4.12))

$$\begin{aligned} P_c &= I_{d(rms)}^2 R_{ds(on)} \\ &\approx I_{d(rms)}^2 R_{ds(on)}(25°C)\left\{1+\frac{\alpha}{100}\right\}^{T_j - 25°C} \quad \text{(W)} \end{aligned} \tag{5.48}$$

where α is the temperature coefficient of the on-state resistance, which is positive. A linear resistance approximation of equation (5.48) is accurate above 25°C if α is small, such that P_c can be approximated by

$$P_c \approx I_{d(rms)}^2 R_{ds(on)}(25°C)\left\{1+\alpha(T_j - 25°C)\right\} \quad \text{(W)} \tag{5.49}$$

5.6.4 Drive input device power loss, P_G

A portion of the drive power is dissipated in the controlling junction or, in the case of the MOSFET, in the internal gate resistance. Usually more power is dissipated in the actual external drive circuit resistance. Drive input loss is normally small and insignificant compared with other losses, and can usually be ignored.

Two possible exceptions are:

- One notable exception is in the case of the power GTO thyristor, where continuous gate drive is used to avoid loss of latching or when the holding current is high. The holding current can be 3% of the anode current thus, the gate to cathode junction loss can be included in the total loss calculation for better accuracy. Thus, for a gate junction voltage V_{GC} the gate losses are given by

$$P_g = \delta I_G V_{GC} \tag{5.50}$$

  The recovery loss of the gate commutated thyristor (GCT) cathode junction can be included since it is significant because the full anode current is extracted from the gate, thus is involved in recovery of the cathode junction.

- A second exception is the MOSFET and IGBT at high switching frequencies, >50kHz, when the loss in the device, associated with providing the gate charge Q_T is given by equation (4.36):

$$P_G(R_{\text{int}}) = V_{gg} Q_T f_s \frac{R_{G\,\text{int}}}{R_{G\,\text{int}} + R_{G\text{ext}}} \quad \text{(W)} \tag{5.51}$$

5.7 Heat-sinking design cases

Heat-sink design is essentially the same for all power devices, but the method of determining power loss varies significantly from device type to device type. The information given in data sheets, in conjunction with the appropriate equation in Table 5.11, allows the designer to calculate power semiconductor thermal rating for a variety of conditions.
Generally, heatsink design is more readily visualised if a thermal equivalent electrical circuit model approach is adopted, as shown in figure 5.1. The equivalence of parameters is shown in Table 5.10. The examples to follow illustrate the approach.

Table 5.10: Thermal equivalent electrical circuit parameters

thermal parameter			thermo-electric model			magnetic model		
temperature drop	Kelvin	ΔT	potential difference	Volts	ΔV	magneto motive force	Amp-turns	$\mathcal{F}$
power dissipated	Watts	P	current flow	Amps	I	flux	Wb	Φ
thermal resistance	K / W	R_θ	Ohm's resistance	Ohms	R	reluctance	Amp-turns/Wb	$\mathcal{R}$

5.7.1 Heat-sinking for diodes and thyristors

At low switching frequencies (<100 Hz), switching loss can be ignored, so that in the case of rectifying diodes or converter-grade thyristors, 50 to 60 Hz, switching loss can usually be ignored. Fast-recovery power diodes switching at less than 500Hz can also have switching losses neglected at low *VA* levels.

5.7.1i - *Low-frequency switching*
At a given current level I_F and on-time duty cycle δ, on-state power loss can be read directly from the manufacturers' data. Figure 5.17a illustrates loss for square-wave power pulses, while figure 5.17b illustrates loss in the case of half-wave sinusoidal current. Figure 5.17b gives energy loss per cycle, which may be converted to power when multiplied by the sinusoidal pulse frequency.
Thyristor loss due to the current waveform initial rate of rise of current, *di/dt*, can be incorporated and its contribution is added into the manufacturers' conduction loss data for a given device type.

5.7.1ii - *High-frequency switching*
At device operating frequencies greater than about 100 Hz, fast-recovery diodes are normally employed and at about 500Hz, switching losses must be added to the on-state conduction loss. Diode turn-off loss is usually more significant than turn-on loss. Manufacturers provide maximum reverse recovery charge, Q_R, characteristics as shown in figure 5.18. The reverse recovery charge is a linear function of temperature and between the given junction temperatures of 25°C in figure 5.18a and 150°C in figure 5.18b, interpolation of Q_R is used.

The reverse recovery W.s/pulse, J_R, can be approximated by

$$J_R = V_R Q_R \quad \text{(J)} \tag{5.52}$$

where V_R is the reverse voltage applied to the diode just after turn-off. Losses are lower since the diode only supports voltage once peak reverse recovery has occurred (at the peak of the reverse current). The reverse recovery average power loss is given by

$$P_s \approx V_R Q_R f_s \quad \text{(W)} \tag{5.53}$$

The total average power loss is the algebraic sum of the steady-state conduction loss and the recovery loss.

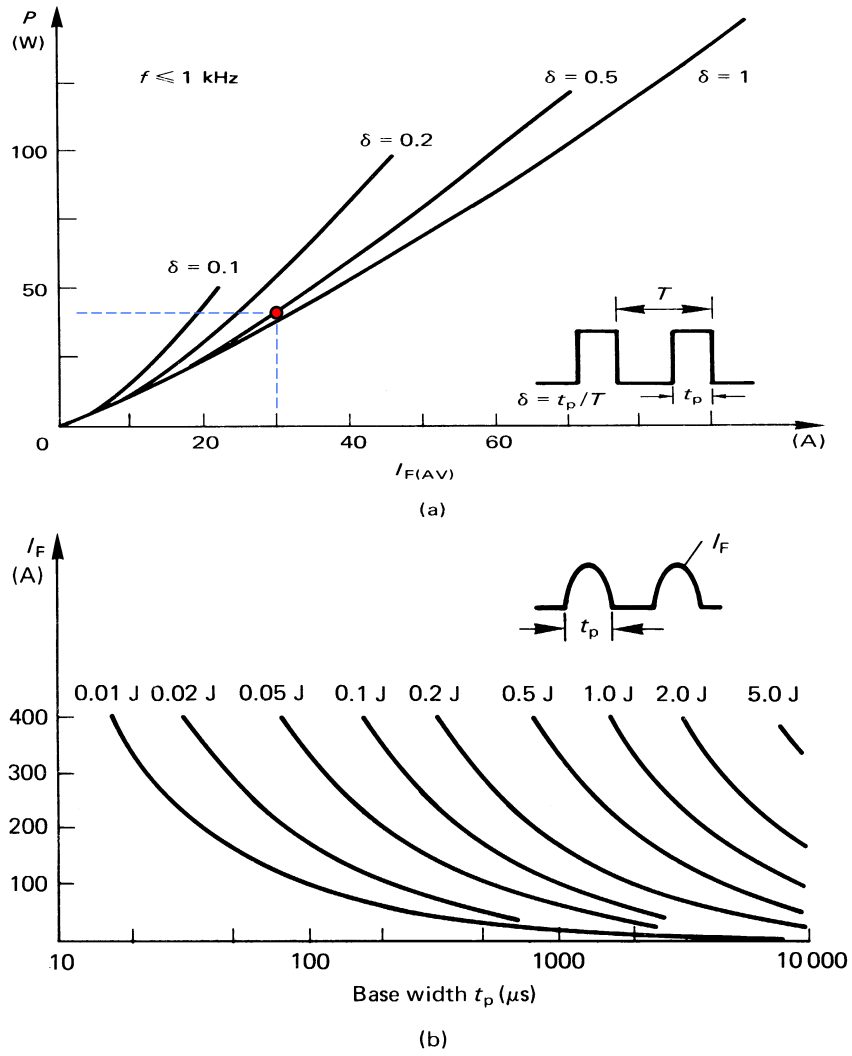


Figure 5.17. *Diode on-state energy loss at low frequency as a function of forward current for: (a) squarewave power pulses and (b) sinusoidal power pulses.*

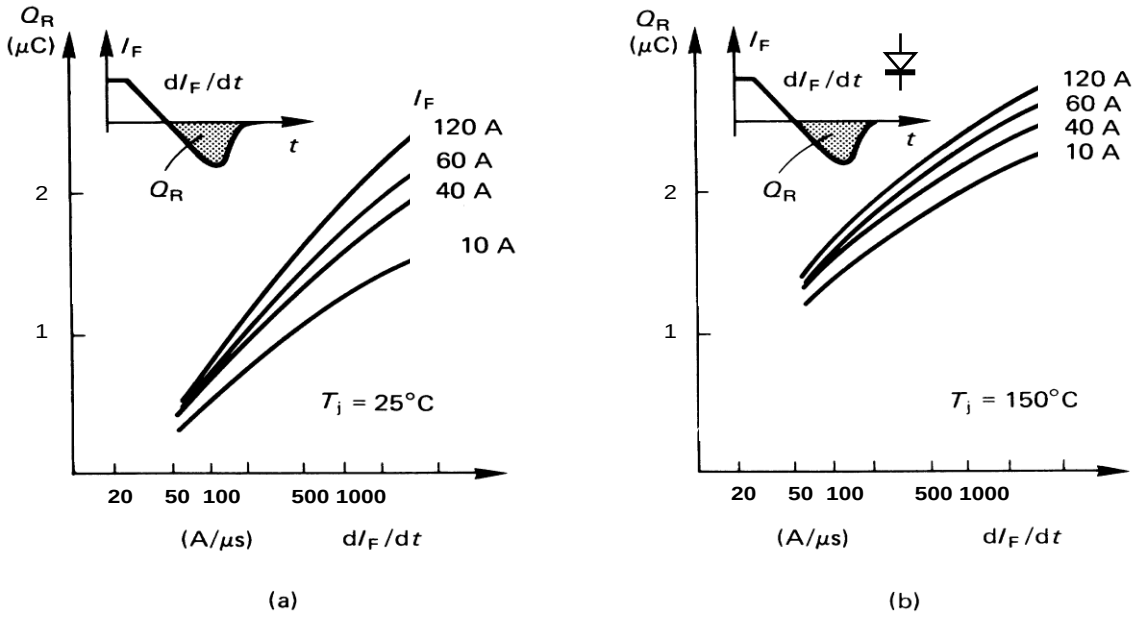
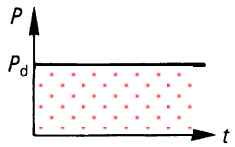
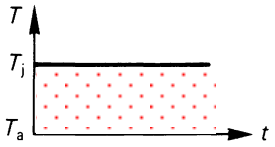
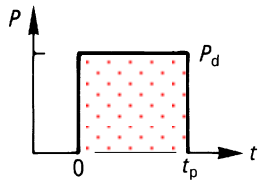
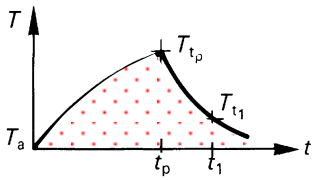
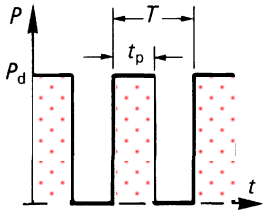
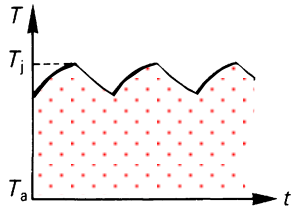
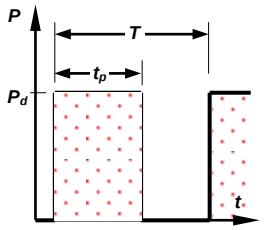
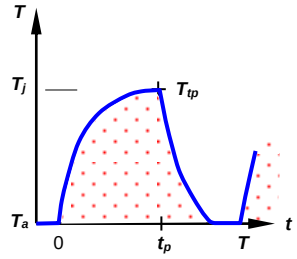
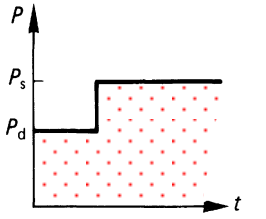
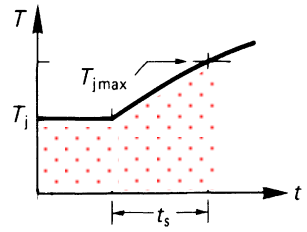


Figure 5.18. *Reverse recovery charge as a function of forward current and dI_F/dt at: (a) 25°C and (b) 150°C junction temperature.*

Table 5.11: Power rating equations based on thermal considerations

Load condition	*Junction power loss waveform*	*Junction temperature rise waveforms*	*Junction temperature solution*
(a) Continuous			$T_j - T_a = P_d R_\theta$
(b) Single pulse			$T_{t_p} - T_a = P_d z_\theta(t_p),\ \delta = 0$ $T_{t_1} - T_a = P_d\{z_\theta(t_1) - z_\theta(t_1 - t_p)\}$
(c) Constant high frequency and constant duty cycle			$\delta = t_p/T$ approximate steady-state solution $T_j - T_a = P_d\{\delta R_\theta + (1-\delta)z_\theta(T + t_p)$ $-z_\theta(T) + z_\theta(t_p)\}$
(d) Constant low frequency and constant duty cycle			$\delta = t_p/T$ $T_{tp} - T_a = P_d z_\theta(t_p)$
(e) Continuous duty followed by a step in power			$T_{jmax} - T_j = P_d R_\theta + (P_s - P_d)z_\theta(t_s)$

Example 5.6: ***Heat-sink design for a diode***

A fast-recovery diode switches 60 A rectangular current pulses at 10kHz. The off-state bias is 400V and the external circuit inductance limits the reverse dI_F/dt to 100A/μs. If the device junction-to-case thermal resistance is 0.7K/W, calculate the minimum heat-sink size requirement with a 50 per cent conduction duty cycle, if the maximum ambient temperature is 40°C.

Solution

The steady-state loss given from figure 5.17a is about 40 W when using $I_{F(AV)}$ = 30A for δ = 0.5.
Minimum possible heat-sinking thermal resistance requirements occur when T_j is a maximum, that is 150°C from figure 5.18b. From figure 5.18b, for dI_F/dt = 100 A/μs and I_F = 60A, the maximum reverse recovery charge is 1.3μC. The switching power loss (over estimate) is given by

$$P_s = Q_R V_R f_s$$
$$= 1.3\mu C \times 400V \times 10kHz = 5.2W$$

The total power loss is therefore

$$P_d = 40 + 5.2 = 45.2W$$

Since the frequency and duty cycle are both high, the concept of thermal resistance is appropriate; that is

$$T_j = T_a + P_d\,(R_{\theta\text{j-c}} + R_{\theta\text{c-a}})$$

Therefore $150\text{V} = 40\text{V} + 45.2\text{A} \times (0.7\Omega + R_{\theta\text{c-a}})$ (in units of the electrical dual)

whence $R_{\theta\text{c-a}} = 1.73$ K/W

Figure 5.6b shows that a minimum of 50mm length of matt black heat sink is required. This assumes that the case-to-sink thermal resistance is negligible. In order to improve device reliability and lifetime, operation at T_j is avoided. A derating of 40 to 50°C significantly reduces junction thermal fatigue and can result in a tenfold improvement in reliability. To restrict T_j to 100°C, $R_{\theta\text{ c-a}}$= 0.7K/W, necessitating 120 mm of the heat sink as characterised in figure 5.6b. The flatness of the $R_{\theta\text{ s-a}}$ curve means that the effectiveness of the heat sink is diminished and either a wider sink of the same length or a shorter length of a profile offering lower thermal resistance would be more effective in reducing device thermal fatigue.

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5.7.2 Heat-sinking for IGBTs

Externally, the IGBT conduction loss is related to the gate voltage and the collector current magnitude, which specify the on-state voltage. No simple power loss characteristic is possible, as in figure 5.17 for the diode and thyristor. Fortunately, the power switching IGBT is used in such a way that its on-state collector-emitter voltage is near constant, whence conduction loss is given by

$$P_c = \delta\, v_{ce} \bar{I}_c \qquad \text{(W)} \qquad (5.54)$$

Example 5.7: ***Heat-sink design for an IGBT- repetitive operation at a high duty cycle***

A power IGBT is used to switch a 20A, 100V inductive load at 10 kHz. The transistor maximum on-state duty cycle is 90 per cent and the device has a junction-to-case thermal resistance of 0.7K/W. The transistor on-state voltage is maintained at 2V and the switch-on and switch-off times are 1 and 2 μs respectively. If the junction temperature is not to exceed 125°C with a maximum ambient temperature of 35°C, what is the minimum heat-sink requirement? Assume that the transistor is in a T0247 package, which is mounted directly on the heat sink but with interface silicone grease used.

Solution

Since both the duty cycle and switching frequency are high, the peak junction temperature is approximated by the average junction temperature. That is, the concept of thermal resistance is valid. The on-state power loss is given by

$$P_c = \delta\, v_{ce} \bar{I}_c = 0.9 \times 2\text{V} \times 20\text{A} = 36\text{ W}$$

From equation (5.45), the switching losses for an inductive load are

$$P_s = P_{s(\text{on})} + P_{s(\text{off})}$$
$$= ½ \times 100\text{V} \times 20\text{A} \times (1\mu\text{s} + 2\mu\text{s}) \times 10\text{ kHz} = 30\text{ W}$$

Total power losses P_d are 36W+30W = 66 W.

From

$$\hat{T}_j = T_a + P_d\left(R_{\theta\text{j-c}} + R_{\theta\text{c-s}} + R_{\theta\text{s-a}}\right)$$
$$125°\text{C} = 35°\text{C} + 66\text{W} \times \left(0.7 + 0.1 + R_{\theta\text{s-a}}\right)$$

Therefore $R_{\theta\text{c-a}} = 0.56$ K/W

The case-to-heat-sink thermal resistance value of 0.1K/W for a T0247 non-insulated case using silicone thermal grease was obtained from Table 5.1. To obtain the minimum heat-sink thermal resistance of 0.56K/W, 150 mm of the heat sink with cross-section shown in figure 5.6a is required. Clearly, a sink profile that has a lower thermal resistance per unit length would be more suitable.

♣

5.7.3 Heat-sinking for power MOSFETs

Switching losses in MOSFETs tend to be low at frequencies below 20 kHz and therefore may be neglected, along with gate and off-state losses. Conduction loss is generally expressed in terms of the on-state resistance as I^2R loss. The first step in the thermal design is to determine the total power dissipation in the device, which is generally dominated by the conduction loss. Determination of this loss is not trivial since, while the power dissipation determines junction temperature, the power dissipation itself is a function of junction temperature, because the on-state resistance increases with temperature, as shown in figure 3.13.

Example 5.8: ***Heat-sink for a MOSFET - repetitive operation at high peak current, low duty cycle***

Find the thermal resistance of the heat sink needed for a MOSFET conducting a repetitive 20A rectangular current waveform. On-time is 10μs, duty cycle is 0.1 per cent, and the maximum ambient temperature is 40°C. Assume $R_{ds\,(on)}$ at 150°C and 20 A is 5 Ohms, and $R_{\theta\,j\text{-}c}$ = 1.5 K/W.

Solution

Since the on-state duty cycle and switching frequency are both low, the peak junction temperature at the end of the on-period will be significantly different from the average junction temperature. The concept of thermal resistance from the junction to the case is therefore invalid; rather the concept of thermal impedance is used.

The peak power per pulse = $P_p = I^2R = 20^2 \times 5\Omega = 2 \times 10^3$ W

Using a thermal impedance basis, the case temperature is given by

$$T_j = T_c + P_p \times Z_{\theta j\text{-}c}$$
$$= T_c + P_p\, r(t_p) R_{\theta j\text{-}c}$$

where $r(t_p)$ is the transient thermal impedance factor for the junction-to-case. For a 10 μs pulse from figure 5.10, $r(t_p)$ = 0.03, assuming δ = 0.001≈ a single pulse condition, thus

$$150°C = T_c + 2\times10^3 \times 0.03 \times 1.5 = T_c + 90°C$$

that is $T_c = 60°C$

The average junction temperature is

$$T_j = T_c + \overline{P}_d R_{\theta j-c} = T_c + \delta P_d R_{\theta j-c}$$
$$= 60°C + 0.1\% \times 2\times10^3 W \times 1.5°C/W$$
$$= 60°C + 3°C = 63°C$$

Although the average junction temperature is only 3°C above the case temperature of 60°C, the peak junction temperature reaches 150°C.

Because of the heat-sink thermal inertia, the concept of thermal resistance and average power are used for calculations involving the heatsink. That is

$$T_c = T_a + \overline{P}_d R_{\theta c\text{-}a} = T_a + \delta P_d R_{\theta c\text{-}a}$$
$$60°C = 40°C + 0.001 \times 2 \times 10^3 \times R_{\theta c\text{-}a}$$

thus $R_{\theta c\text{-}a} = 10$ K/W

The heat sink of cross-section shown in figure 5.6a is not suitable in this application, and one of a much smaller surface area is applicable. A heatsink may not be necessary since the package thermal resistance $R_{\theta\,c\text{-}a}$, shown in figure 5.1, may be less than 10K/W, there in satisfying equation (5.17). See problem 5.6.

♣

If the junction operating temperature is unknown but can be assumed greater than 25°C, from equation (5.49), the total power loss can be expressed as

$$P_d = P_o + I^2_{d(rms)} R_{ds(on)}(25°C)\left\{1 + \alpha(T_j - 25°C)\right\} \quad (W) \qquad (5.55)$$

where P_o represents all losses other than the conduction loss, and is assumed temperature independent. The temperature coefficient α for $R_{ds\,(on)}(25°C)$ is positive, typically 1 per cent/K as indicated in figure 3.13. The usual thermal equality holds, that is

$$T_j = T_a + R_{\theta j\text{-}a}\, P_d \quad (K) \qquad (5.56)$$

Combining equations (5.55) and (5.56) by eliminating T_j yields

$$P_d = \frac{P_o + I^2_{d(rms)} R_{ds(on)}(25°C)\left\{1 + \alpha(T_a - 25°C)\right\}}{1 - I^2_{d(rms)} R_{ds(on)}(25°C)\alpha R_{\theta j\text{-}a}} \quad (W) \qquad (5.57)$$

The denominator yields an asymptotic maximum drain current of

$$I_{d(\text{rms})} = \frac{1}{\sqrt{R_{ds(\text{on})}(25°\text{C})\ \alpha\ R_{\theta\text{j-c}}}} \quad \text{(A)} \qquad (5.58)$$

at which current thermal runaway would result. In practice, insufficient gate voltage is available and the device would leave the constant-resistance region and enter the constant-current region, where the above analysis is invalid.

Example 5.9: ***Heat-sink design for a MOSFET - repetitive operation at high duty cycle***

A power MOSFET switches 5 A rms at 10 kHz with a maximum on-state duty cycle of 90 per cent. The junction-to-case thermal resistance is 0.7 K/W, the maximum ambient temperature 35°C, and on-state resistance at 25°C is 1 Ohm. If the heat-sink arrangement yields an effective case-to-ambient thermal resistance of 1.3 K/W and α = 0.01 /K, what is the junction operating temperature?

Solution

Since the switching frequency and duty cycle are both relatively high, the thermal resistance concept based on average junction power dissipation is valid.

Assuming zero losses other than conduction losses, then P_o = 0. Equations (5.55) and (5.56) rearranged to eliminate P_d yield

$$T_j = \frac{T_a + R_{\theta\text{j-a}} I^2_{d(\text{rms})} R_{ds(\text{on})}(25°\text{C})\{1 - 25\alpha\}}{1 - \alpha R_{\theta\text{j-a}} I^2_{d(\text{rms})} R_{ds(\text{on})}(25°\text{C})} \quad \text{(W)} \qquad (5.59)$$

Assuming typical α = 0.01/K and $R_{\theta\,\text{j-a}} = R_{\theta\,\text{j-c}} + R_{\theta\,\text{c-a}}$

$$T_j = \frac{35°\text{C} + 2 \times 5^2 \times 1\Omega \times (1 - 25 \times 0.01)}{1 - 0.01 \times 2 \times 5^2 \times 1\Omega} = 145°\text{C}$$

♣

Example 5.10: ***Two thermal elements on a common heatsink***

A dc chopper has a MOSFET switch that dissipates 40W and a load freewheel diode that dissipates 20W. Each power device is mounted on a common heatsink. The MOSFET has a junction-to-case thermal resistance of 0.7K/W and a case-to-heatsink thermal resistance of 0.5K/W. The diode has a junction-to-case thermal resistance of 0.8K/W and a case-to-heatsink thermal resistance of 0.6K/W.

i. Determine the maximum heatsink thermal resistance that maintains both junction temperatures below 90°C in a 30°C ambient.

ii. Semiconductor lifetime approximately doubles for every 10°C decrease in junction temperature. If the heatsink in the previous case is fan cooled, estimate the lifetime improvement if the heatsink thermal impedance is halved with fan cooling.

iii. If the load current is constant (25A) and the switch and diode on-state voltages are the same, determine the chopper on-time duty cycle and device instantaneous losses assuming no switching losses (only on-state losses).

Solution

i. Applying Kirchhoff's voltage law to each loop of the equivalent thermal circuit shown gives:

$$T_{Dj} - T_{hs} = 20\text{W} \times (0.8\text{K/W} + 0.6\text{K/W}) = 28°\text{C}$$

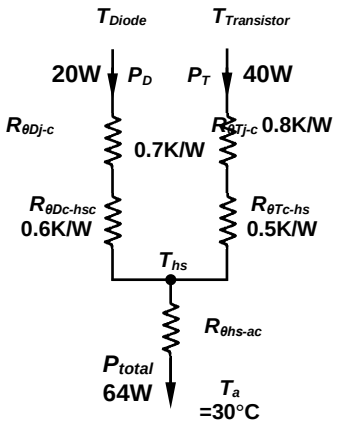
$$T_{Tj} - T_{hs} = 40\text{W} \times (0.7\text{K/W} + 0.5\text{K/W}) = 48°\text{C}$$

Since both semiconductor devices are mounted on the same heatsink, T_{hs} is the same in each case, the MOSFET virtual junction will operate 20°C hotter than the diode junction. Therefore the MOSFET junction temperature should not exceed 90°C, that is

$$90°\text{C} - T_{hs} = 40\text{W} \times (0.7\text{K/W} + 0.5\text{K/W}) = 48°\text{C}$$

giving a heat sink surface temperature of 90°C - 48°C = 42°C and a diode junction temperature of 42°C + 28°C = 70°C. The heatsink thermal resistance requirement is

$$T_{hs} - T_a = 42°C - 30°C = R_{\theta hs-a} \times (40W + 20W)$$
$$R_{\theta hs-a} = \frac{42°C - 30°C}{40W + 20W} = \frac{12°C}{60W} = 0.2K/W$$



ii. Assume device losses are not affected by temperature and the heatsink thermal resistance is decreased to ½×0.2 = 0.1 K/W, then

$$T_{hs} - T_a = T_{hs} - 30°C = 0.1K/W \times (40W + 20W)$$
$$T_{hs} = 0.1K/W \times (40W + 20W) + 30°C = 36°C$$

The device junction temperatures are given by

$$T_{Dj} - 36°C = 20W \times (0.8K/W + 0.6K/W) \text{ that is } T_{Dj} = 64°C$$
$$T_{Tj} - 36°C = 40W \times (0.7K/W + 0.5K/W) \text{ that is } T_{Tj} = 84°C$$

The junction temperature of each device has decreased by about 6°C, so although the lifetime will have increased, lifetime improvement is not doubled. Device package thermal properties are more dominant than the heatsink in determining junction temperatures.

iii. If the on-state duty cycle is δ and the instantaneous device losses are both P (since the on-state voltage is the same for both devices and the current is constant hence the same for both when each device conducts) then

mosfet $\quad \delta P = 40W$
diode $\quad (1-\delta)P = 20W$

Summing these two equations gives an instantaneous loss of P = 60W, whence a switch on-state duty cycle of $\delta = \frac{2}{3}$, that is the switch conducts for 66$\frac{2}{3}$% of the cycle period. The diode on-state voltage is therefore 60W/30A = 2.0V and the MOSFET on-state resistance is 60W/30A^2 = 67mΩ.

♣

Example 5.11: ***Six thermal elements (on a common substrate) in a common package***

A three-phase full-wave diode rectifier package consists of six-diode die within a single module. The junction-to-case thermal resistance of each die is 0.24K/W. The module is mounted on a heatsink with a module-to-heatsink contact thermal resistance of 0.2K/W and a heatsink-to-ambient thermal resistance of 0.1K/W. The maximum ambient temperature is 30°C and the highly inductive load current is constant at 100A. If the diode on-state voltage is 1V, determine

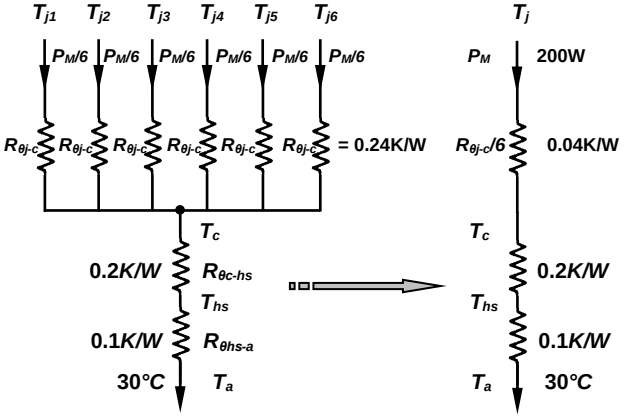
i. the diode junction temperature
ii. the current to double the rectifier lifetime (decrease junction temperature by 10°C)
iii. the heatsink to double the rectifier bridge lifetime (at 100A).

Solution

i. During rectification, two diodes always conduct therefore total module conduction losses are

$$P_M = 2 \times I_o \times V_{Don} = 2 \times 100A \times 1V = 200W$$

The figure shows how the six thermal paths can be reduced to the simplified equivalent thermal model on the right.



Applying Kirchhoff's voltage law

$$T_j - T_a = P_M \times \left(\tfrac{1}{6} R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a}\right)$$
$$T_j - 30°C = 200W \times \left(\tfrac{1}{6} \times 0.24K/W + 0.2K/W + 0.1K/W\right)$$
$$\Rightarrow \quad T_j = 98°C$$

ii. If the current is reduced so as to decrease the diode junction temperature by 10°C then

$$T_j - T_a = P_M \times \left(\tfrac{1}{6} R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a}\right)$$

$$88°C - 30°C = P_M \times \left(\tfrac{1}{6} \times 0.24K/W + 0.2K/W + 0.1K/W\right) \quad \Rightarrow \quad P_M = 170.6W$$

Assuming the diode on-state voltage drop is independent of current, that is remains 1V then

$$P_M = 2 \times I_o \times V_{Don}$$

$$170.6W = 2 \times I_o \times 1V \quad \Rightarrow \quad I_o = 85.3A$$

iii. When the junction temperature is reduced by 10°C to 88°C by decreasing the heatsink thermal resistance, and the constant load current is maintained at 100A

$$T_j - T_a = P_M \times \left(\tfrac{1}{6} R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a}\right)$$

$$88°C - 30°C = 200W \times \left(0.04K/W + 0.2K/W + R_{\theta hs-a}\right) \quad \Rightarrow \quad R_{\theta hs-a} = 0.5K/W$$

♣

Reading list

Fishenden, M. and Saunders, 0. A., *An Introduction to Heat Transfer,* Oxford University Press, 1982.

http://www.electronics-cooling.com

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http://www.lytron.com/

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http://www.1-act.com/

http://pcmproducts.net/

5.8 Appendix: Comparison between aluminium oxide and aluminium nitride (substrates)

Aluminium Nitride is made by nitridation of aluminium or by conversion of alumina Al_20_3 to aluminium nitride. It is a covalently bonded material and has a hexagonal crystal structure. Because of its resistance to sintering, an oxide-forming additive such as Y_20_3 is needed to form a substrate. General comparison properties of aluminium oxide and nitride are listed in Table 5.12.

Aluminium nitride is a cost effective, non-toxic alternative to beryllium oxide and has a thermal conductivity nearly eight times higher than alumina (aluminium oxide). Advantages of aluminium nitride include good thermal performance, low thermal expansion, and non-toxicity. Aluminium nitride offers:

- High thermal conductivity
- Low thermal expansion coefficient closely matching silicon
- Good dielectric strength
- High electrical sensitivity
- Low toxicity and therefore excellent replacement for Be0
- Good shock and corrosion resistance
- Low dielectric loss
- High temperature stability
- High flexure strength and light weight
- Resistant to wafer processing gasses and plasma erosion
- Conducive to finishing operations such as lasering, lapping, and polishing
- Substrate for direct bond copper DBC and filled vias
- Good adhesion for thin and thick film applications
- Uniform lapped and polished surfaces for resistor networks
- Polished and lapped surface finishes to 12nm, R_a, with minimum pullouts
- Lapped surface finishes to 150nm, R_a, where is the roughness average profile

$$R_a = \frac{1}{n}\sum_{i=1}^{n}\left|y_i\right|$$

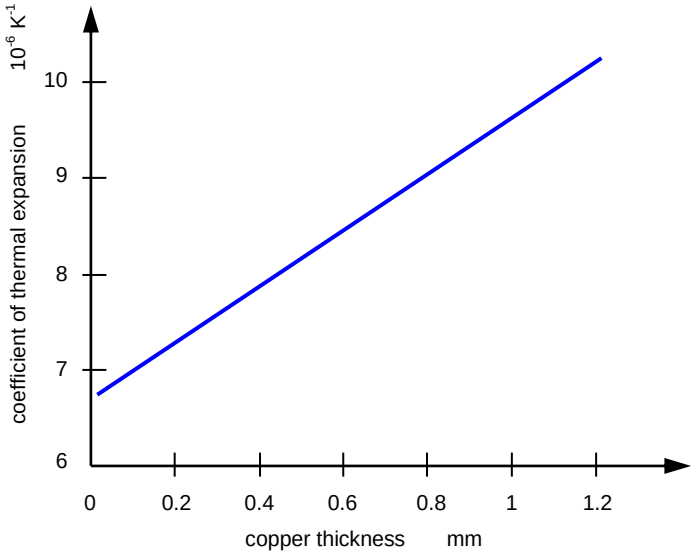
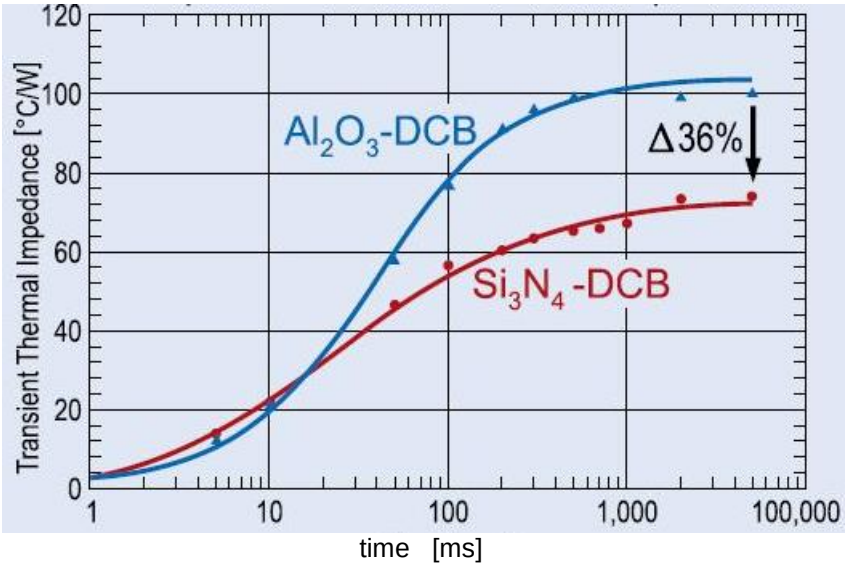


Figure 5.19. *Thermal expansion dependence on copper base plate thickness.*

Table 5.12: Substrates properties

Material		Aluminium nitride	Aluminium oxide	Beryllium oxide	Silicon carbide
symbol		$A\ell_3N_4$	$A\ell_2O_3$		
Colour		Tan/Gray	white	white	
Melting point/ maximum use temperature	°C	>2200/800 oxidizing	2054/1700	2507/1800	-/1650
Purity	wt %	98%	99.6%	99.5	
Density	g/cm^3	>3.25	>3.65	2.85	3.2
Thermal Conductivity	W/m. K	100 - 300	27	265	270
Thermal Expansion	x10^{-6}/K @ >20°C	<4.3	<7.7	8.0	3.7
Specific Heat	J/kg K	740	880		750
Dielectric Strength	kV/mm	>15	>12	9.5	
Dielectric Constant	at 1MHz @ 20°C	8.7	9.2	6.6	40
Dissipation Factor	x10^{-4} @ 1 MHz)	3 - 7	3	4	
Volume Resistivity	ohm-cm	>10^{14}	>10^{12} at 20°C >10^8 at 500°C	10^{15}	10^2-10^6
Flexural Strength	kg$_f$ /mm MPa	>250 300	>280 345	120-150 150-200	450 550
Modulus of elasticity	GPa	331	372	345	410
Hardness (Knoop)	GPa	11.8	14.1	9.8	27
Poisson's ratio		0.22	0.21	0.26	0.14
toxicity		nontoxic	nontoxic	toxic	nontoxic
Substrate Specification					
Maximum Dimension	mm	140 x 100mm,	100 x 200		
Thickness	mm	0.63 - 0.2 mm	0.63 - 0.30mm		
Surface Roughness	micron	as fired - 0.3 as lapped - 0.075 as polished - 0.025	as fired - 0.3 as lapped - 0.075 as polished - 0.025	as fired - 0.3 as lapped - 0.1 as polished-0.08	

At room temperature, the thermal conductivity of aluminium nitride ceramics is independent of $A\ell_3N_4$ grain size or number of grain-boundaries, but is controlled by the internal structure of the grains, such as the degree of oxidation (oxygen contamination). Thermal impedance is compared in the following figure.



The coefficient of thermal expansion for direct copper bonded (DCB) substrates with a layer of 0.6 mm alumina sandwiched between Cu layers of various thicknesses is shown in figure 5.19.

5.9 Appendix: Properties of substrate and module materials

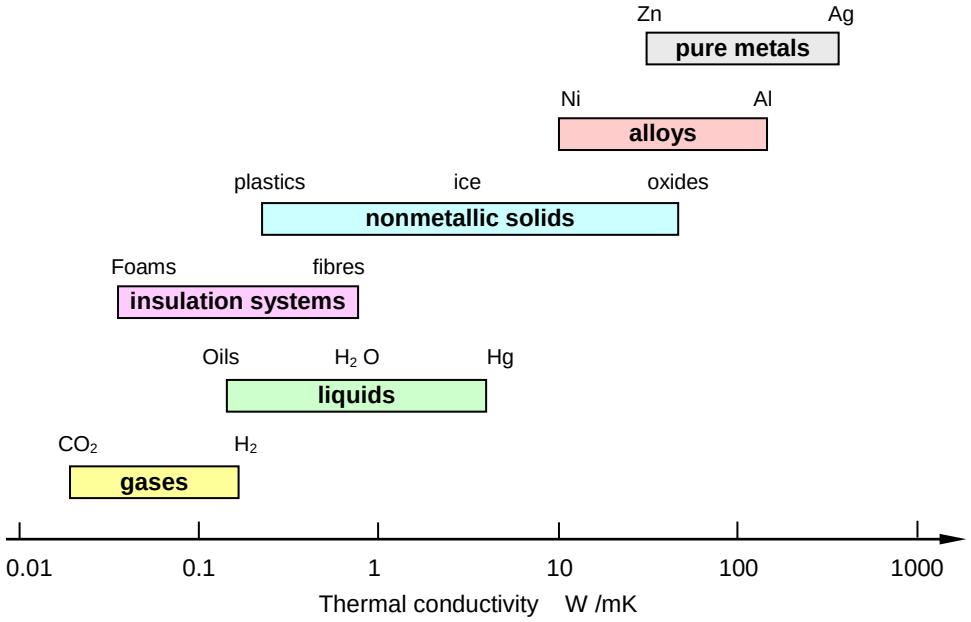


Table 5.13: Substrate characteristics

Material	Al_2O_3, BeO, AℓN, Quartz, Silicon, Sapphire, Ferrite
Surface Finish	Al_2O_3 As Fired, 0.05µm maximum;
Polished	to 0.12µm
Dimensions	0.5mm x 0.5mm to 100mm x 100mm
Dimensional Tolerance	± 0.01mm scribed; (± 0.002mm saw cut)
Thickness	0.012mm inches to1.2mm
Thickness Tolerance	0.12mm standard to as tight as 0.04mm
Sputtered Resistor Material	NiCr, Ta_2N Sputtered Metallization Ti, TiW, Pd, Ni, Au, Aℓl
Electro-Plated Metals	Au, Cu, Ni, Solder
Electroless Plated Metals	Sn, Ni, Au

Table 5.14: Properties of module materials

material	relative permittivity	dielectric loss factor	specific thermal conductivity	linear thermal expansion coefficient	temperature coefficient of ε_p	type
	@1MHz	10GHz, 25°C		@25°C		
	ε_r	$tan\delta_\varepsilon$	λ	$\Delta l / l \ / \Delta T$	$\Delta\varepsilon / \varepsilon \Delta T$	
		$\times 10^{-4}$	W/m K	10^{-6}/K	10^{-6}/K	
$A\ell_20_3$ 99.5%	9.8	1	37	6.5	136	insulator
sapphire	9.4	1	42	6	110	insulator
Quartz glass	3.78	1	1.7	0.55	13	insulator
Beryllium oxide ceramic Be0	6.3	60	210	6.1	107	insulator 8900kg/m^3
GaAs	12.9	20	46	5.7		semiconductor
Silicon $\rho = 10^3$ Ωcm	11.9	150	145	4.2		semiconductor
PTFE	2.2	3	0.2	106	350	plastic
polyolefin	2.32	7	0.5	108	480	plastic
copper	1.0		393	17	24.1	metal
aluminium	$-1300+j1.3\times10^{14}$		220	23.8		metal

Table 5.15: Power electronic component properties

material		thermal conductivity	specific heat capacity	density	temperature coefficient of expansion	Melting point
20°C		λ	c	ρ_ℓ	CTE	
		W /m K	J/ kg K	kg/m^3	ppm/K	K
air (STP)		0.026	1004	1.2	-	
silicon	Si	120	700	2330	3.5	1685
solder	PbSn	50	150	8400	24.1	183
copper	Cu	385	385	8930	17	1358
alumina	$A\ell_20_3$	22	80	3720	6.5	
aluminium nitride	$A\ell_3N_4$	170	725	3300	4.5	
aluminium silicon carbide	AℓSiC	170		3000	7	
polyimide		0.2	1100	1400		
dielectric layer		0.3	1400	1120		
encapsulation		0.5		2000		
aluminium	Aℓ	205	900	2710	22.5	775
gold	Au	315	126	19320	14.2	1336
platinum (90%) Iridium (10%)		31.1				
platinum	Pt	70.9	1448	21450	9.0	1728
tungsten	W	188	130	19300	4.6	3410
molybdenum	Mo	140	250	10200	4.9	2610
lead	Pb	235	130	11340	23	327
tin	Sn	66	227	7300	23	232
Cu/Mo/Cu					5.8	
silicon carbide	SiC	700	250	3.21	3.7	
sapphire		2700	419	3900	8.4	2040
diamond		2300	509	3500	2.4	3100
brass	CuZn	111	343	8490	18.0	920
steel (low carbon)		48	460	7850	11.5	1370
Mica K Mg_3 $AlSi_3$ O_{10} $(OH)_2$		0.6				1700

beryllium	Be	230	1088	2880	5.9	1280
silicon thermal grease		0.8	2093	2.8	-	
thermal conducting plastic		20				

5.10 Appendix: Emissivity and heat transfer coefficient

Emissivity is not only a material property but also a surface property, at least for opaque materials. Consequently, coatings (oxides, grease, and water film) influence the value measured under pristine conditions. For example, the emissivity of a copper surface covered with 2 µm oxide increases from 0.03 to 0.2. In practice, surfaces that are initially shiny are covered with oxide and dust after one year of operation. Additionally, surface texture can influence the emissivity because of a strong dependence on angle.

For heat transfer calculations, total hemispherical emissivity is found by integration over all wavelengths and all angles. What is being measured with an IR camera is the normal spectral emissivity restricted to the wavelength band of the detector.

As a rule of thumb: for unpolished metals the ratio of hemispherical to total emissivity is 1.1 to 1.3, and for non-conductors 0.95 to 0.97. Another angle-dependent difference between metals and insulators is that under a shallow incident angle, the emissivity of metals tends to one and insulators tend to zero.

A complication is, the emissivity of many materials of interest is strongly dependent on the wavelength. That is, there is a big difference between the visible band and most common IR bands (0.8 to 3 µm, 3 to 8 µm, 8 to 14 µm). Si and Ge are notorious examples. It is relevant to low-temperature applications (<100°C) because the bulk of the radiation is in the long-wavelength region: 8 to 14 µm. This is the main reason why the colour of paints is not relevant for heat sinks and casings. All colours are black. Apart from the fact that it is simply impossible to account for all the physics of radiation in a practical situation, the problem is only relevant when radiation is an important contribution to the total heat transfer. For natural convection cases, this contribution might well be 40%. When the choice is between an emissivity of 0.05 and 0.1, the radiation contribution is 2 to 4% - minimal. When the choice is 0.7 to 0.9, matters are different. Most heat transfer simulation software that support radiation heat transfer, assume the following simplifications:

- surfaces diffuse, grey (sometimes specula [mirror-like]), opaque
- surfaces isothermal
- surfaces uniformly irradiated
- medium is transparent for all relevant wavelengths

In summary, differences exist between experimental data and simulation results when radiation is a major factor, even when all other data are known to within 1%.

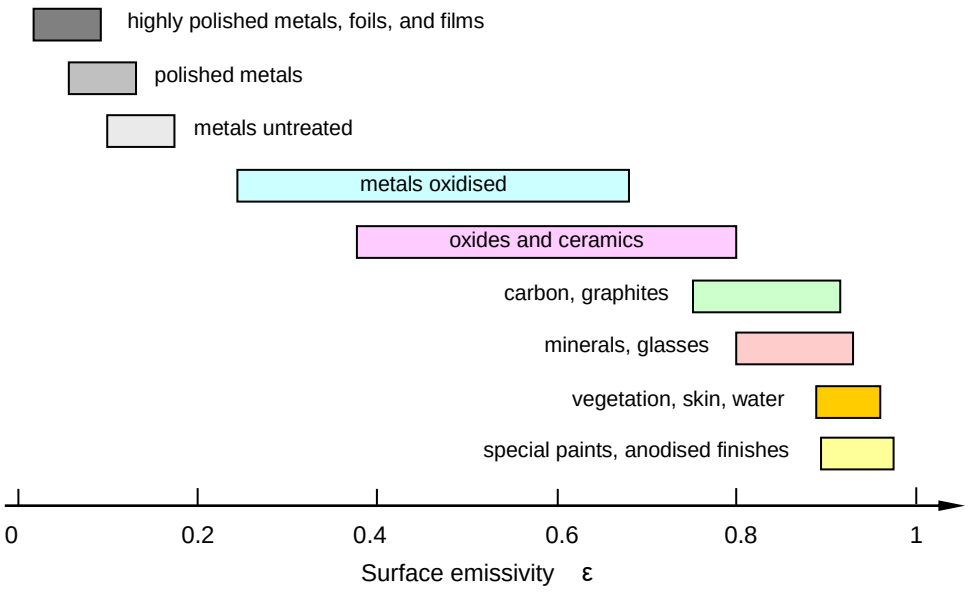
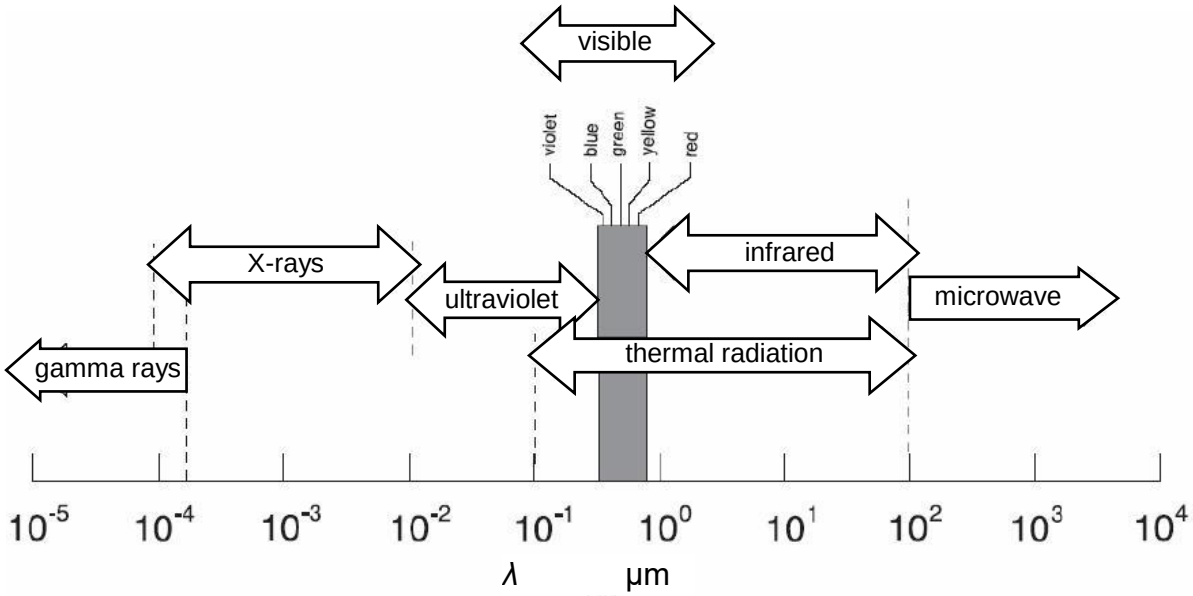


Table 5.16 shows typical material normal total emissivity values at 20°C.

Table 5.16: Normal total emissivity values @ 20°C

Metals		ε	**Coatings**	ε
Aluminium	polished	0.04	Aluminium bronze	0.3
	sheet	0.09	Aluminium paint	0.35
Brass	polished	0.05	Blackbody paint	0.97
	oxidized	0.22	Enamel	0.82
Chromium	polished	0.06	Lampblack	0.95
	rough	0.74	Paint	0.89
Copper	polished	0.03		
Gold	polished	0.025	**Various**	
Graphite	polished	0.42	Glass, Quartz	0.93
Inconel	polished	0.2	Ice	0.98
Iron	polished	0.06	Plastics	0.8
	oxidized	0.85	Paper	0.8
	ground	0.24	Porcelain	0.92
	cast	0.16	Silk, Cotton, Wool	0.75
Mercury		0.09	Stone	0.8-0.9
Molybdenum	polished	0.05	Water (> 0.1mm)	0.95
	@ 2600 K	0.29	Wood	0.9
Silver	polished	0.025		
Steel	polished	0.06		
	oxidized	0.6		
Silicon	difficult	0.3 - 0.8		
Tin	bright	0.07		
Tungsten	polished	0.05		



Electromagnetic spectrum

Natural convection heat transfer coefficient

The convective heat transfer coefficient h, for various geometry arrangements are given by equations (5.60) and (5.61), as applicable, in conjunction with Table 5.17.

$$h = k_h \left(\frac{\Delta T}{D} \right)^{1/4} \tag{5.60}$$

$$h = k_h \left(\frac{\Delta T}{L} \right)^{1/4} \tag{5.61}$$

where ΔT is temperature difference, K
L is length, m
D is diameter, m

Table 5.17: Heat transfer coefficient constant, k_h

Geometry	Dependant geometrical parameter		constant k_h	equation
Vertical cylinder or plate	Vertical height L		1.42	(5.61)
Horizontal cylinder	Diameter D		1.32	(5.60)
Horizontal plate	$L = \frac{4 \times area}{perimeter}$	Upper surface hot	1.32	(5.61)
		Lower surface hot	0.59	
Vertical populated PCB	Vertical height L		2.44	(5.61)
Sphere	Diameter D		1.92	(5.60)

5.11 Appendix: Ampacities and mechanical properties of rectangular copper busbars

Effect of emissivity and number of busses on ampacity (current carrying capacity) – data in Table 5.18 shows how higher emissivities improve ampacity. Multiple busses also affect ampacity in a nonlinear relationship. Ampacity may be raised by increasing heat dissipation with convection cooling or surface treatments. Surface treatments which improve emissivity are oxidation or thinly coated, flat, inorganic based spray paints.

Table 5.18: Ampcapacity

number of 6mm x 100mm busses	Ampacity, A											
	30°C rise				50°C rise				65°C rise			
	emissivity ε				emissivity ε				emissivity ε			
	0.15	0.4	0.7	0.9	0.15	0.4	0.7	0.9	0.15	0.4	0.7	0.9
1	1100	1250	1400	1600	1500	1700	1900	2000	1700	1950	2200	2300
2	1900	2050	2200	2300	2550	2750	2950	3100	2950	3200	3400	3600
3	2500	2700	2850	3000	3400	3600	3850	4000	3950	4200	4500	4600
4	3100	3300	3450	3600	4200	4400	4700	4800	4900	5100	5400	5600
6mm spacing. Ampacities of bus bar systems of other configurations must be calculated taking into account size, spacing, number of bus bars, and overall skin-effect ratio.												

5.12 Appendix: Isolated substrates for power modules

Currently used isolated substrates for power modules are:

Isolation material

Ceramic: aluminium oxide Al_2O_3
aluminium nitride AlN
(beryllia oxide Be0)
(silicon nitride Si_3N_4)

Organic: epoxy
polyimide (Kapton)

Substrates

Metal sheets: *DCB* (**D**irect **C**opper **B**onding) AMB (**A**ctive **M**etal **B**razing)

Metal sheets: IMS (**I**nsulated **M**etal **S**ubstrate) Multilayer-IMS

Thick film layers: TFC (**T**hick **F**ilm **C**opper)

*DCB (**D**irect **C**opper **B**onding)*

Power modules with IGBTs (or MOSFETs) and freewheel diodes commonly use substrates made of *DCB*-ceramics with $A\ell_20_3$ or $A\ell N$ isolation that combine good thermal conductivity and high isolation voltage.

For DCB, copper surfaces 200µm to 600µm thick, typically 300µm, are applied to the top and bottom surfaces of the isolation substrate material (0.25mm to 0.85mm thick, typically 0.5mm) by eutectic melting at between 1065°C and 1083°C. The sandwiched copper oxide layer helps adjust for the different thermal expansion rates. After the necessary track structure for the module circuitry has been etched into the top side copper surface, the chips are soldered on, and contact connection on the chip top side is effected by bonding. The bottom side copper of the DCB-ceramic substrate is fixed to the module base plate (about 3mm thick copper) usually by soldering, as seen figure 5.8. Other module types do not necessarily require a base plate and the soldering procedure may be avoided.

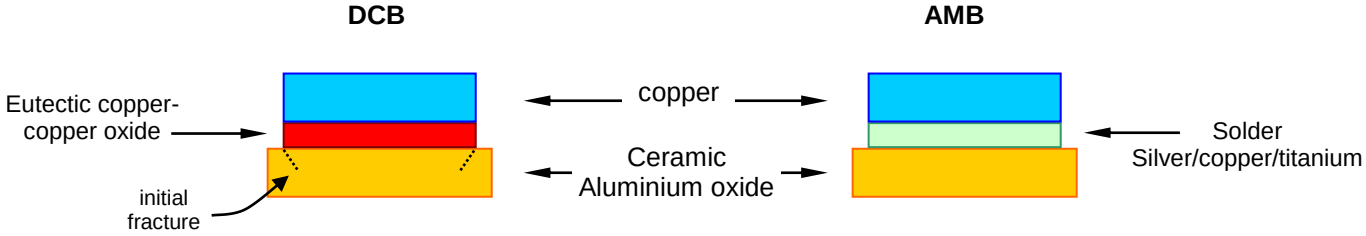


Figure 5.20. *Direct copper bonding, DCB and active metal brazing, AMB.*

Advantages of the DCB-technology compared to other structures are mainly the high current conductivity due to the copper thickness, good cooling features due to the ceramic material, the high adhesive strength of copper to the ceramic (reliability), and the optimal thermal conductivity of the ceramic material. Possible failure due to cracking, termed conchoidal fracture, starts at the copper edge, as shown in figure 5.20, and progressively extends under the copper interface area.

*AMB (**A**ctive **M**etal **B**razing)*

The AMB process (*brazing* of metal foil to a substrate) has been developed based on DCB technology. The advantages of AMB-substrates with $A\ell N$-ceramic materials compared to substrates with $A\ell_20_3$-ceramic materials are lower thermal resistance, lower coefficient of expansion, and improved partial discharge capability.

Figure 5.20 illustrate the differences between DCB and AMB. AMB offers higher partial discharge levels than DCB.

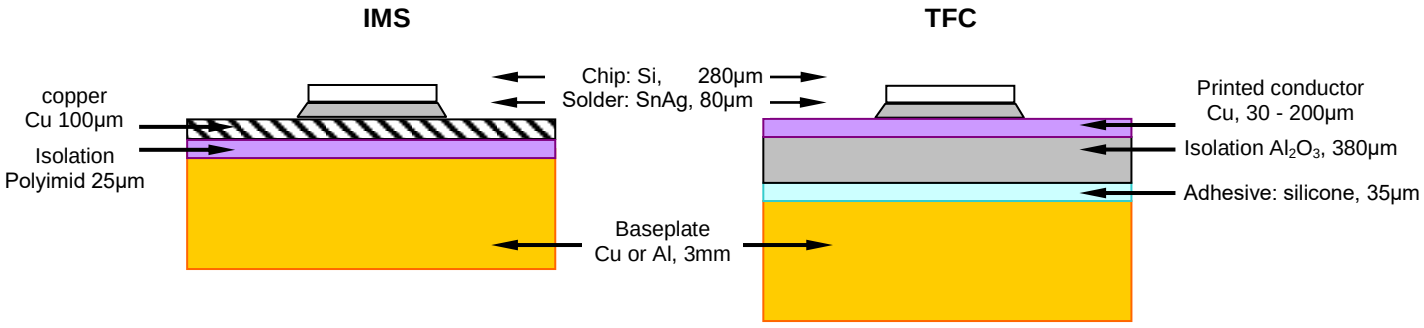


Figure 5.21. *Basic module structure of: (a) an IMS power module and (b) a TFC power module.*

*IMS (**I**nsulated **M**etal **S**ubstrate)*

IMS is mainly used in the low-cost, low-power range and is characterized by direct connection of the isolation material to the module base plate. For insulation, polymers (such as epoxies, polyamides) are applied to an aluminium base plate, as seen in figure 5.21a. The upper copper layer is produced in foil form and glued onto the isolation substrate (similar to PCB production) and is patterned by etching.

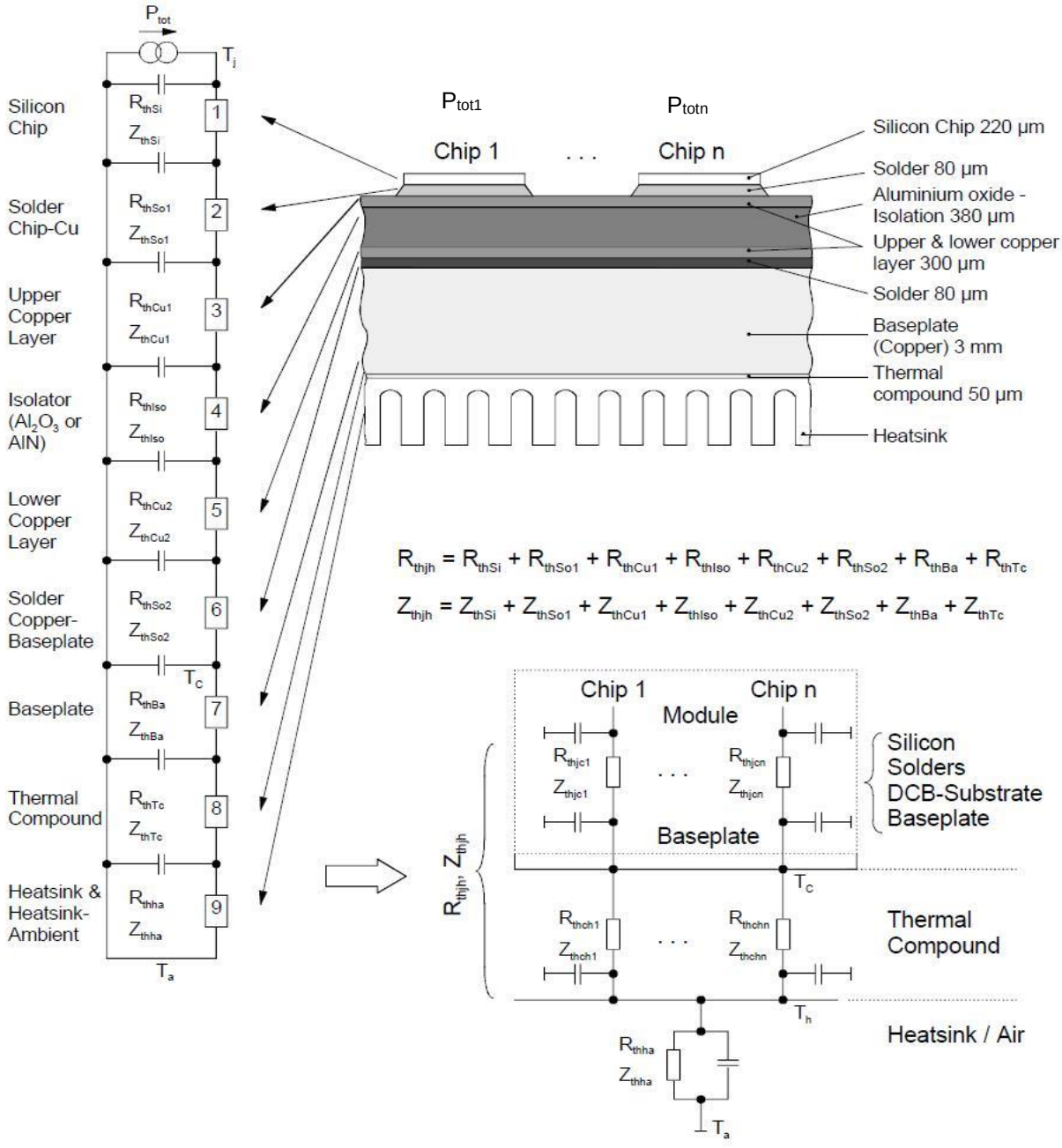
Advantages of IMS are low costs, filigree track structure (possible integration of driver and protection

circuitry), substrate high mechanical robustness, and relatively wide substrate areas, compared to DCB. The thin isolation layer, however, leads to comparably high coupling capacitances associated with the mounting surface. Also the thin upper copper layer only provides a comparably low heat spreading, which is improved by additional metallised heat spreading layers under the chips or by adding Aℓ-particles to the isolation layer.

*TFC (**T**hick-**F**ilm-**C**opper)-thick film substrates*

Just as with DCB, the basic material for thick film substrates is an isolation ceramic, which is glued directly onto the base plate or a heatsink by means of silicone or applied by soldering, as shown in figure 5.21b. The tracks on the top of the ceramic substrate are made of copper and are applied by screen printing. The power semiconductor chips or other components are soldered or glued onto the track pads.

TFC technology can also be combined with standard thick film technology. Since low resistances may be produced by the paste materials which are usually applied in thick film technology, and since isolated tracks can be arranged on top of one another and connected together, quite a number of system components may be densely integrated. However, the filigree tracks, typically 15µm thick, limit the current capability of such structures to about 10A.



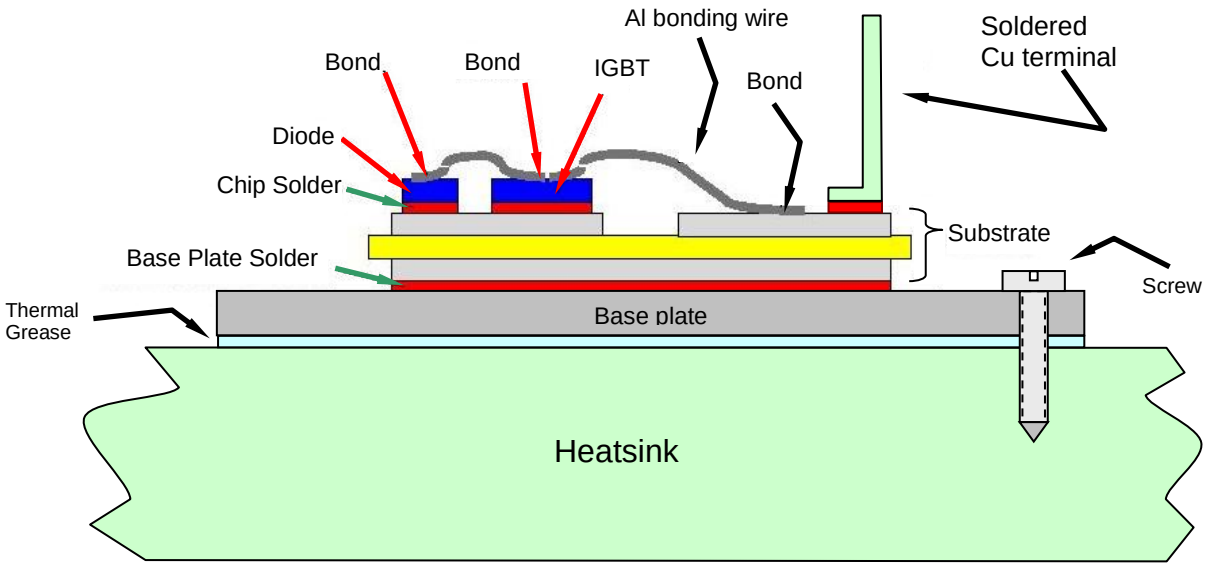


Figure 5.22. *Power module with DCB substrate: (a) basic structure and (b) thermal model.*

High-temperature lead-free transient liquid phase (TLP) die and substrate attach methods

While silicon semiconductor technology is limited to junction temperatures of about 200°C, emerging SiC technology could exploit 600°C operating temperatures, were it not for die and substrate attachment limitations and aluminium thermal bonding stressing.

The high-temperature, lead-free silver-tin transient liquid phase (TLP) die attach process for connecting the SiC power devices to a nickel-plated direct bond copper (DBC) or direct bond aluminium (DBA) power substrate (aluminium nitride or silicon nitride) shown in figure 5.23a, allows junction temperature operation in excess of 400°C.

Similarly the high-temperature, lead-free nickel-tin TLP attachment process for connecting the nickel-plated DBC or DBA power substrate to a metal matrix composite, MMC, base-plate allows operation to temperatures in excess of 400°C.

The baseplate of the power module can utilize a lightweight copper-molly (CuMo) metal matrix composite (MMC) that has a coefficient of thermal expansion (CTE) characteristic closely matching that of the SiC power die. This CTE matching reduces thermal-stress mismatches, thus improving the long-term thermal stressing reliability of a power module. The common use of copper as base plate material is for its advantages of high thermal conductivity, easy mechanical handling, galvanic plating and acceptable pricing. Disadvantages are non-reversible changes of mechanical properties above 300°C and the mismatch of the coefficient of thermal expansion (CTE) to the ceramic substrate. The mismatch of the CTEs is Cu (17ppm/K) and AℓN (7.3ppm/K). Due to this mismatch thermal stress occurs between the materials and generates mechanical strain on the solder. AlSiC is an alternative baseplate material for significantly improved thermal cycling properties.

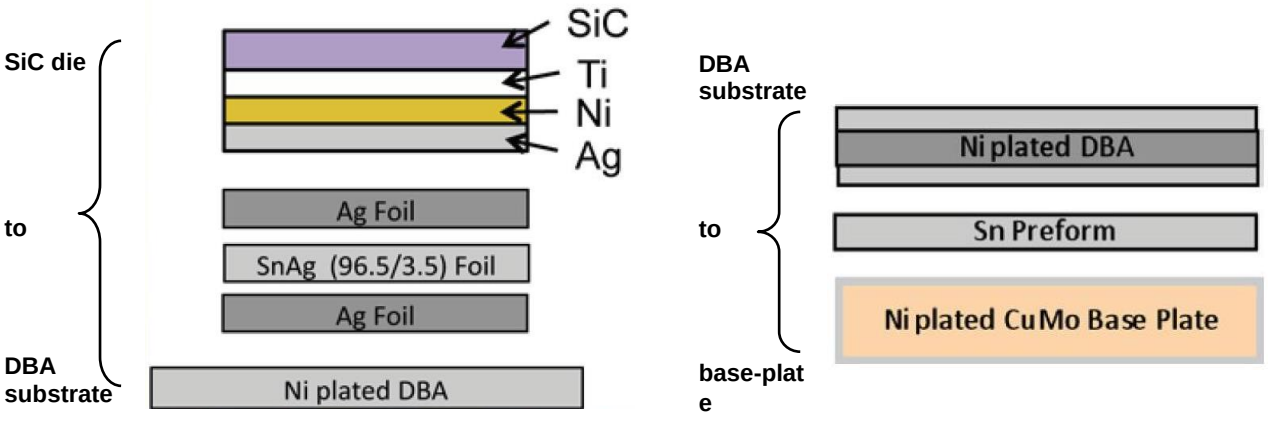


Figure 5.23. *Cross-section of various layers in the lead-free 400°C high temperature SiC power module: (a) Ag-Sn TLP die attach and (b) Ni-Sn TLP substrate attach.*

Problems

5.1. A thyristor bridge switches at 1 kHz and the total energy losses per thyristor are 0.01 Joule per cycle. The thyristors have isolated studs and a thermal resistance of 2 K/W. The heat sink has a thermal resistance of 1.8 K/W. Calculate the maximum number of thyristors that can be mounted on one heat sink if the thyristor junction temperature is not to exceed 125°C in an ambient of 40°C. What is the heat sink temperature?

[3 devices, T_s= 94°C]

5.2. A transistorised switch consists of two IGBTs and two 1 Ohm current-sharing resistors, as shown in figure 5.24, mounted on a common heat-sink. Each transistor has a thermal resistance $R_{\theta j\text{-hs}}$ of 2 K/W, while each resistor has a thermal resistance $R_{\theta\ r\text{-hs}}$ of 1 K/W. The maximum switching frequency is 1 kHz and the maximum duty cycle is 99.99 per cent. The heat-sink thermal resistance $R_{\theta\ hs\text{-a}}$ is 1 K/W. The energy losses per transistor are 5 mJ/A per cycle. If the ambient temperature is 30°C, maximum allowable junction temperature is 150°C, and the maximum allowable resistor internal temperature is 100°C, calculate the switch maximum current rating based on thermal considerations. What are the operating temperatures of the various components, assuming ideal current sharing?

[6.88 A, T_r = 100°C, T_{hs} = 88°C, T_j = 122.5°C]

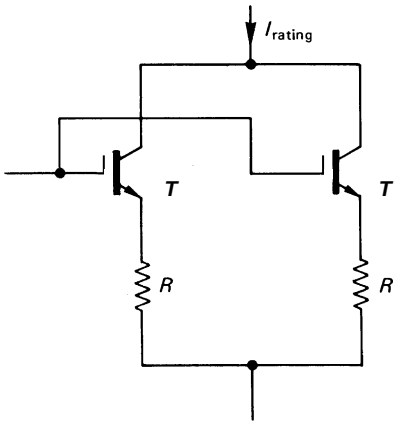


Figure 5.24. *Problem 5.2.*

5.3. Figure 5.25a shows the circuit diagram for a power current sink which utilises a 40V source. Both the IGBTs *T* and wire wound resistors *R* are mounted on a common heat-sink, of thermal resistance $R_{\theta\ hs\text{-a}}$ = 1 K/W. The transistor has a thermal resistance of 2 K/W from the junction to the heat-sink, and 10 K/W from the junction to air via the transistor casing exposed to the air. The resistor has a mounting thermal resistance from the insulated wire to the heat-sink of 1 K/W and 10 K/W from the wire to the air via its casing exposed to the air. The maximum transistor junction temperature is 423 K, the maximum resistor wire temperature is 358 K and the ambient air temperature is 303 K.

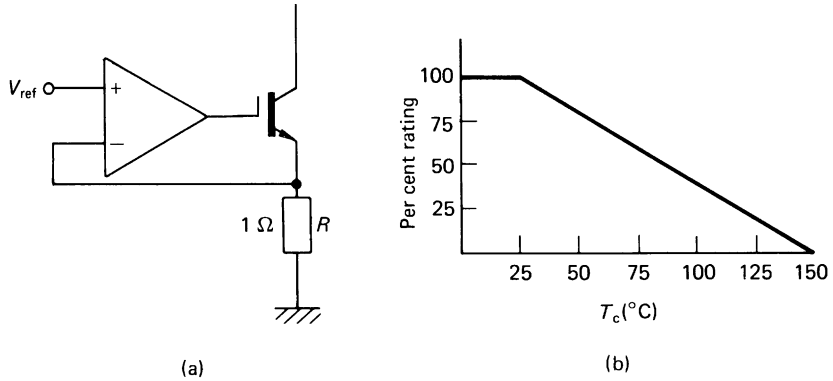


Figure 5.25. *Problem 5.3.*

Based on thermal considerations, what is the maximum current rating of the current sink and under such conditions, what is the heat-sink temperature?
What power rating would you suggest for the 1 Ohm current measurement resistor?
Are there any difficulties in operating the transistor in the linear region in this application if it is in a 120 W dissipation package which is derated according to figure 5.24b?

[1.36 A, 69°C, > 2 W]

5.4. A power IGBT switches a 600 V, 25 A inductive load at 100 kHz with a 50 per cent on-time duty cycle. Turn-on and turn-off both occur in 100 ns and the collector on-state voltage is to be 2 V.
Calculate the total power losses, P_d, of the switch.
The switch has a thermal resistance $R_{\theta j\text{-hs}}$ = 0.05 K/W, and the water-cooled heatsink provides a thermal resistance $R_{\theta hs\text{-w}}$ = 0.05 K/W. Calculate the operating junction temperature if the water for cooling is maintained at 35°C.
The 25 A steady state load current is stepped to 200 A. Calculate the surge power dissipation P_s, at 200 A, assuming transistor switching and on-state characteristics remain unchanged.
The junction temperature for a power surge during steady-state operation is given by case (e) in Table 5.11.
With the aid of figure 5.10, determine the junction temperature at the end of a 0.1s, 200 A pulse. How long is it before the junction temperature reaches T_j = 125°C, with a collector current of 200 A?
(Assume $R_{\theta c\text{-hs}}$ = 0).

[175 W, 52.5°C, 1400 W, 112.6°C, 0.5 s]

5.5 Rework example 5.6 finding the case temperature when the switching losses equal the on-state loss.

5.6 A 20kHz, step-down, 340V dc chopper feeds an inductive load with an average current of 20A and a peak-to-peak ripple of 20A. Thus the MOSFET switch on-state current rise from 10A to 30A while the freewheel diode current falls from 30A to 10A when the switch is off. The MOSFET on-state resistance is 0.1Ω and has switch on and off times of 100ns and 200ns respectively. The switch duty cycle is 75% and it has a thermal resistance $R_{\theta j\text{-}c}$ of 0.4K/W and is mounted on a heatsink of thermal resistance $R_{\theta c\text{-}a}$ of 0.6K/W in a maximum ambient temperature is 40°C.
Calculate:

i. switching losses, using equations 7.9 and 7.10
ii. switch on-state losses
iii. MOSFET junction operating temperature

[3.4W + 20.4W = 23.8W; I_{rms} = 15.8A, 25W; T_j = 88.8°C]