CHAPTER 4

Electrical Ratings and Characteristics of Power Semiconductor Switching Devices

Semiconductor device characteristics and ratings are primarily concerned with electrical and thermal properties. The thermal properties and cooling design aspects are similar for all power switching semiconductor devices. A common, unified thermal design approach is applicable since manufacturers use the concept of a semiconductor device being thermally represented by one *virtual junction*. This virtual junction is considered as the point source of all losses, which comprise on-state and off-state losses as well as switch-on and switch-off losses and any control input loss.

Not only are the power dissipation characteristics similar for all semiconductor devices, but many similarities exist in the area of maximum device ratings.

4.1 General maximum ratings of power switching semiconductor devices

The maximum allowable limits of current, applied voltage, and power dissipation are defined as the *maximum ratings* for that device. These absolute maximum ratings are important and the device must not experience a condition under which any one limit is exceeded if long life and reliability are to be attained. Generally, at worst, the device should experience only one near maximum rating at any instant.

Ratings are dependent on the materials used, the structure, the design, the mount, and the type of processes employed. The one property inherent in these physical features is temperature dependence and its interaction on electrical properties. Maximum ratings are therefore generally based on the variation of electrical characteristics that arises from the created variations. Because of this close correlation between properties, different ratings cannot be considered independently. Also, ratings are highly dependent on the device external circuit conditions.

This interdependence of device properties and the effects of external circuit conditions are no more evident than during *thermal runaway* - a condition to be avoided. Such a condition can occur in all devices that have bipolar junctions. For example, with the diode, thyristor, and the MOSFET's parasitic diode; reverse recovery current increases junction temperature. The reverse recovery charge increases with temperature, thus increasing junction power dissipation and further raising the junction temperature. This endless increasing of temperature and recovery charge results in thermal runaway and eventual device destruction. A similar thermal runaway condition occurs in the bipolar transistor and devices employing BJT mechanisms, like the thyristor and the IGBT. Here, collector current causes an increase in temperature which increases the conductivity of the bipolar transistor. More current then flows, further increasing the device temperature. If external circuit conditions allow, thermal runaway occurs, eventually resulting in irreversible device damage.

Figure 4.1 shows the electrical operating bounds of common semiconductor power switches, where the general trend is the higher the *I-V* ratings the slower the possible switching frequency, (because of increased losses associated with attaining higher sustaining voltages), hence increased junction temperature. High-frequency low-power switching applications are dominated by the MOSFET or possibly trench-gate IGBTs while high-power low-frequency switching applications are dominated by thyristor type devices or possibly IGBT modules. Rectifying or fast recovery diodes, as appropriate, are available with matched *I-V* ratings for all the switch device types in figure 4.1.

4.1.1 Voltage ratings

The absolute voltage limit is characterised by a sharp increase in leakage current when the device has at least one junction reverse-biased. The most commonly experienced voltage-limiting mechanism is that of avalanche multiplication, as considered in chapters 2.2.2 and 3.1.2. Since leakage current increases significantly with increased temperature, as shown in figure 2.2 and given by equation (2.7), the absolute repetitive voltage rating must be assigned such that thermal runaway does not occur. Most voltage ratings, because of historic reasons, are characterised at an impractical case temperature of 25°C. The leakage current at rated voltage and 25°C varies from hundreds of microamperes for low voltage devices (less than 600V) to milliamperes for high voltage devices (> 3.3kV).

4.1.2 Forward current ratings

The current limit is that value at which the device reliability or functionality is impaired, either in the short term or long term. The forward current ratings are specified after consideration of the following factors.

- Current at which the junction temperature does not exceed a rated value.
- Current at which internal leads and contacts are not evaporated.
- External connector current-handling capabilities.

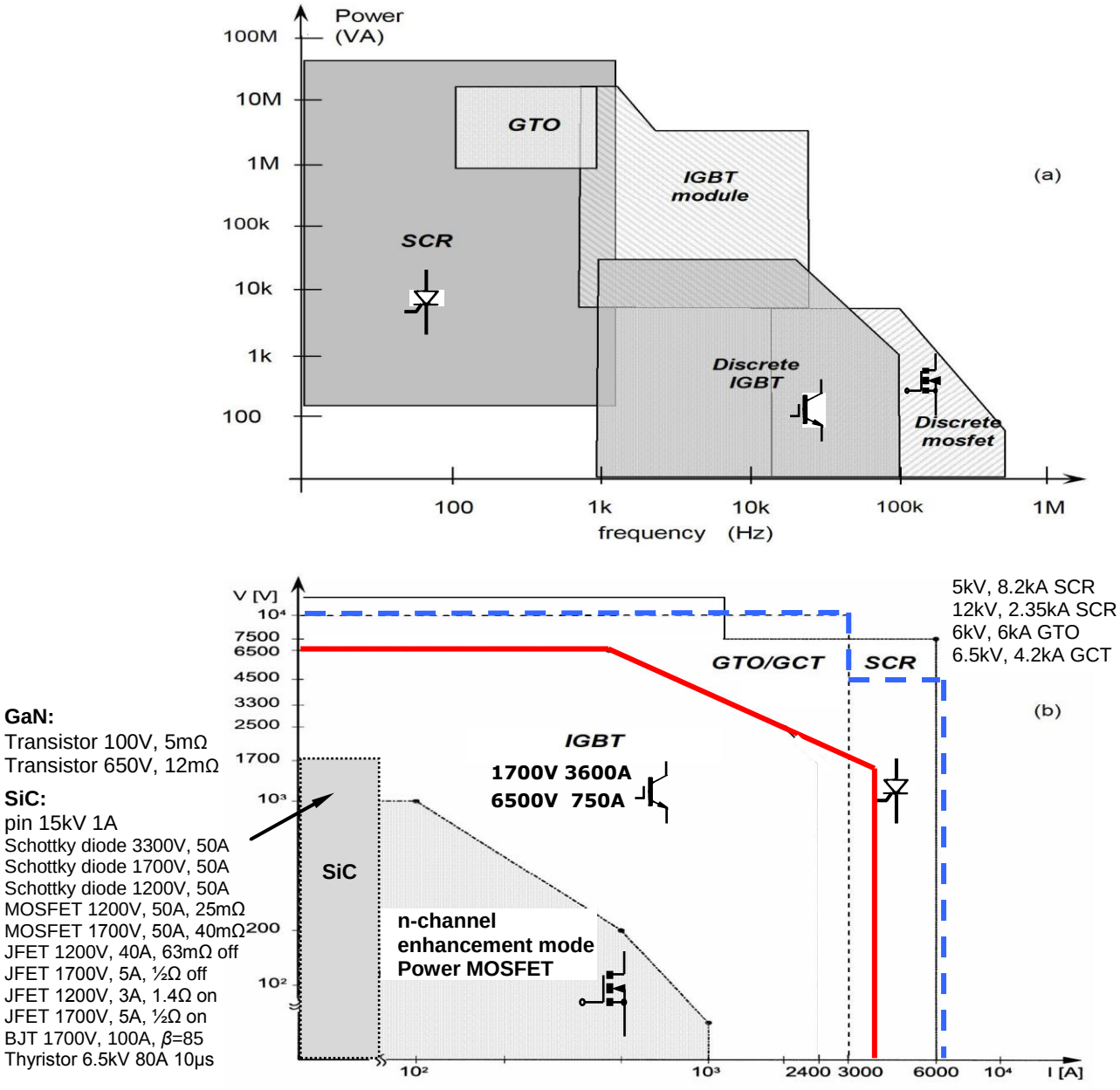

Figure 4.1. *Electrical rating bounds for power switching silicon based devices, where (a) frequency related losses limit upper power through-put and (b) voltage is restricted by silicon limitations while current is bounded by packaging and die size constraints.*

4.1.3 Temperature ratings

The maximum allowable junction temperature $\hat{T}_j$, is dependent on the quality of the materials used and the type of junction, and is traded off against the reduced reliability that arises from deterioration and accelerated service life. The higher the junction temperature, the higher the rate of deterioration. The relationship between service life L_t in hours, and the junction temperature T_j (K) is approximated by

$$\log_{10} L_t \approx A + B / T_j \tag{4.1}$$

where A and B are constants which are related to the device type.

4.1.4 Power ratings

Power dissipated in a semiconductor device is converted into thermal energy which produces a temperature rise. The major parameters limiting the maximum allowable power dissipation $\hat{P}_d$ are maximum allowable junction temperature and device case temperature T_c. These parameters are related to one another by the *thermal resistance* R_θ, according to

$$\hat{P}_d = \frac{\hat{T}_j - T_c}{R_{\theta \text{j-c}}} \quad \text{(W)} \tag{4.2}$$

The virtual junction to case thermal resistance $R_{\theta\,\text{j-c}}$ is a physical value representing the ratio, junction temperature rise per unit power dissipation. Thermal resistance is a measure of the difficulty in removing heat from the junction to the case. Most maximum power values are specified at a case temperature of 25°C, and are derated linearly to zero as the case-operating temperature increases to $\hat{T}_j$, which is typically a maximum of 175°C and 200°C for silicon and silicon carbide power devices, respectively.

4.2 The fast-recovery diode

Static I-V diode characteristics were considered in Chapter 2 and Chapter 3.1. In low-frequency applications the only problem posed by a rectifier is heat dissipation, which can be readily calculated if the current waveform is known. On the other hand, calculation of losses in rectifiers for high-frequency application requires knowledge of device switching phenomena. The forward and reverse recovery characteristics are the most important fast-recovery bipolar pn diode electrical switching properties.

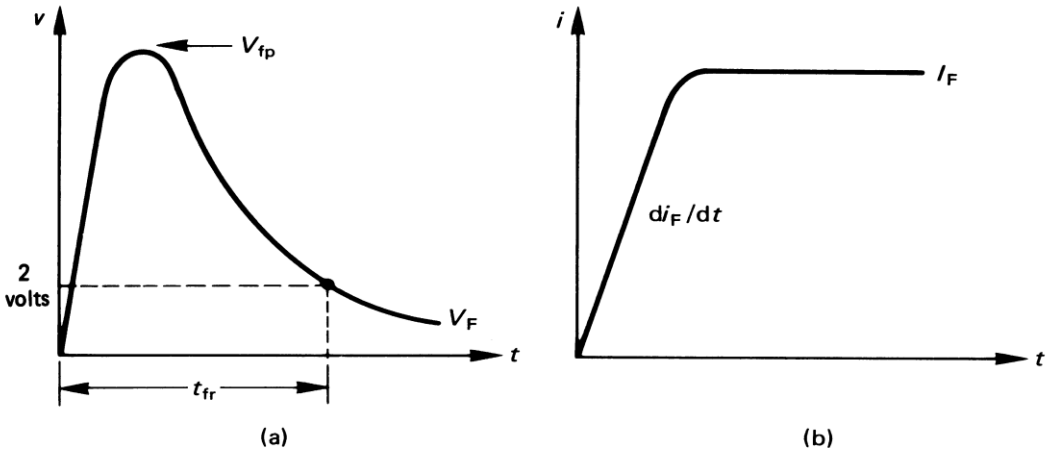

Figure 4.2. *Diode forward recovery measurement: (a) specification of forward recovery time, t_{fr} and peak forward voltage, V_{fp} and (b) diode anode current test waveform.*

4.2.1 Turn-on characteristics

During the forward turn-on period of a rectifier, an overshoot voltage is impressed in a forward bias direction across the diode as the forward current increases. The forward recovery characteristics of time t_{fr} and peak forward voltage V_{fp} are measured as shown in figure 4.2, with a specified increase in forward current di_F/dt, rising to a maximum forward current level I_F.

Two mechanisms predominate and contribute to the forward voltage overshoot phenomenon. The first mechanism is resistive, while the second is inductive.

Initially at turn-on, the device resistance is dominated by the ohmic resistance of the low-concentration n-region. As the concentration of the injected minority carriers increases, the n-region becomes conductively modulated and the associated ohmic voltage drop decreases significantly. These charging effects contribute to a minor initial capacitive component which serves to clamp V_{fp} initially to zero.

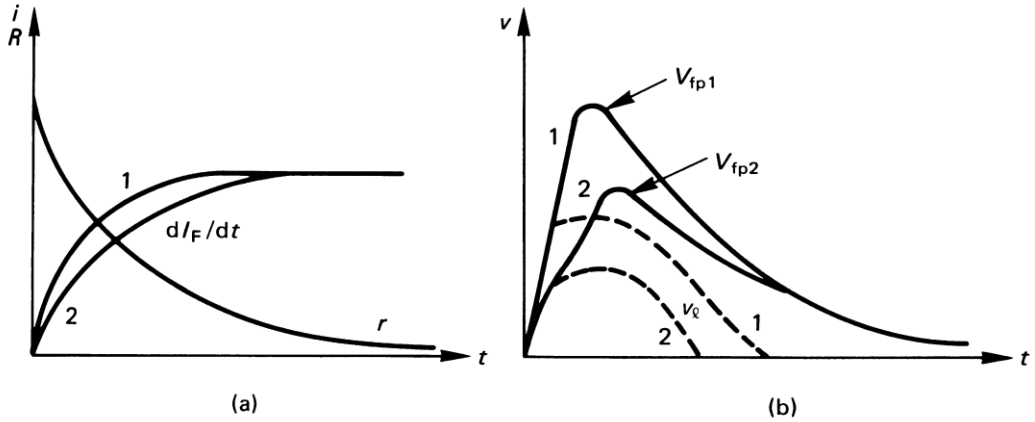

Figure 4.3. *Diode forward turn-on characteristics for two initial anode di/dt cases: (a) forward current and effective change in resistive component, r and (b) anode voltage and voltage contribution v_ℓ, as a result of die inductance.*

The forward di_F/dt causes a voltage drop across the internal device inductance. This inductance comprises both the diode wafer internal inductance and the bonding and connection inductance. In bipolar power devices, the inductance of the wafer predominates. Any inductance contribution to the forward transient voltage ceases when the steady-state current level I_F is reached, as shown in figure 4.3. It will be seen that the peak forward transient voltage increases as di_F/dt increases. The resistive component predominates at low di_F/dt.

As with most minority carrier based power semiconductor characteristics, the turn-on phenomenon is significantly worsened by an increase in junction temperature. That is, both t_{fr} and V_{fp} increase with increased temperature. Although a pre-reversed biased junction condition does not significantly prejudice the turn-on characteristics, if the junction is pre-forward biased slightly, the turn-on transitional phase can be significantly reduced. The Schottky diode, a majority carrier device, does not suffer from forward turn-on transient effects. Package inductances and junction capacitance dominate at turn-on.

4.2.2 Turn-off characteristics

When a forward-conducting bipolar junction diode is abruptly reverse-biased, a short time elapses before the device actually regains its reverse blocking capabilities. Most importantly, before the diode does regain blocking ability, it may be considered as a short circuit in its normally blocking direction.

During forward conduction there is an excess of minority carriers in each diode region and the holes in the n-region and electrons in the p-region must be removed at turn-off. The attempted reverse bias results in a reverse current flow as shown in figure 4.4.

The total *recovery charge* Q_Σ is given by

$$Q_\Sigma = \tau I_F \tag{4.3}$$

where I_F is the forward current before switching. In the usual p^+n diode, the excess minority holes in the n-region are more dominant. The lifetime τ is therefore the hole lifetime τ_h. Since carrier lifetime increases with temperature, recovery charge increases with temperature.

The recovery charge Q_Σ has two components, one due to internal excess charge natural recombination and the other, the *reverse recovery charge* Q_R, due to the reverse diode current shown in figure 4.4.

The excess charges reside in the neutral scl regions of the diode that border the junction. The excess charge concentration is largest at the scl edge on the n-side, reducing to zero well before the cathode contact.

Turn-off is initiated at t_f and the reverse recovery current i_{rr} commences. The rate of rise of this current is determined solely by the external inductance L of the switching circuit and the circuit applied reverse voltage E, according to

$$\frac{dI_F}{dt} = -\frac{E}{L} \quad \text{(A/s)} \tag{4.4}$$

Until the time t_o, the diode carries forward current and is forward-biased. When the current reverses, the forward voltage drop decreases slightly but the device still remains positively biased. The external

circuit inductance *L* supports the voltage *E.* The excess carrier concentrations now begin to reduce as holes leave via the junction, in providing the reverse current, i_{rr}. Holes are therefore extracted first and quickest at the edge of the scl.

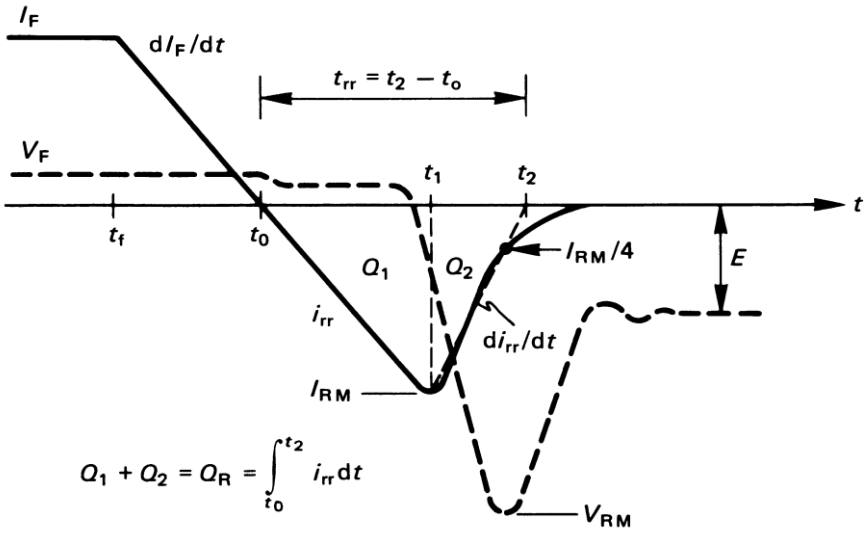

Figure 4.4. *Diode voltage and current during reverse recovery at turn-off.*

At time t_1, the hole concentration at the scl edge reaches zero, the charge Q_1 has been removed (plus natural recovery) and charge Q_2 remains. The reverse current now reduces rapidly since insufficient holes exist at the scl edge. The scl widens quickly, as it is charged. That is, the diode regains its ability to support reverse voltage and at the maximum reverse current I_{RM}, dI_F/dt reduces to zero.

Since $dI_F/dt = 0$, the voltage across the circuit inductance *L* drops rapidly to zero and *E* is applied in reverse bias across the diode. Between t_1 and t_2 the rate of change of reverse current di_{rr}/dt is high and, in conjunction with *L,* produces a reverse voltage overshoot to V_{RM}. After time t_2, di_{rr}/dt reduces to zero, the circuit inductance supports zero volts, and the diode blocks the external circuit voltage *E.*

In specifying the *reverse recovery time,* $t_{rr} = t_2 - t_0$, the time t_2 is defined by projecting i_{rr} through $¼I_{RM}$ as shown in figure 4.4. The reverse recovery time t_{rr} and peak reverse recovery current I_{RM}, at high magnitude dI_F/dt such that $Q_R \approx Q_\Sigma$, are approximated by

$$t_{rr} \approx 2.8 \times 10^{-6}\ V_b\sqrt{I_F / |dI_F/dt|} \quad \text{(s)}$$
$$\text{and} \qquad I_{RM} \approx 2.8 \times 10^{-6}\ V_b\sqrt{I_F \times |dI_F/dt|} \quad \text{(A)} \qquad (4.5)$$

where the avalanche breakdown voltage for a step junction, V_b, is given by equation (2.3). The reverse recovery charge Q_R is therefore given by

$$Q_R = ½ I_{RM} t_{rr} = 3.92 \times 10^{-12}\ V_b^2\ I_F \quad \text{(C)} \qquad (4.6)$$

that is, the reverse recovery charge is proportional to the forward current, as shown in figure 5.18a for dI_F/dt >100 A/μs.

Figure 4.5 illustrates *snap-off* and *soft recovery* diode properties (S_r) which are characterised by the recovery di_{rr}/dt magnitude. The higher the value of di_{rr}/dt, the higher is the induced diode overshoot V_{RM} and it is usual to produce soft recovery diodes so as to minimise voltage overshoot V_{RM}, resulting from inductive ringing.

Reverse recovery properties are characterised for a given temperature, forward current I_F, and dI_F/dt as shown in figure 5.18.

4.2.3 Schottky diode dynamic characteristics

Being a minority carrier device, the Schottky barrier diode, both in silicon and silicon carbide, is characterised by the absence of forward and reverse recovery, plus the absence of any temperature influence on switching.

Forward recovery traits tend to be due to package and external circuit inductance.

Reverse recovery is dominated by the barrier charging – a capacitive effect, which increases slightly with increased temperature, reverse *di/dt*, and I_F. The barrier charge requirements are significantly less than the highly temperature dependant minority carrier charge Q_Σ, associated with the bipolar pn junction diode. Unlike the pn diode, as Schottky junction charging occurs, the junction reverse bias voltage begins to increase immediately. Turn-off voltages are well controlled, less snappy, as the scl capacitor barrier junction acts like a capacitive turn-off snubber, as considered in chapter 9.3.

Whereas the transient performance is virtually independent of temperature, the static forward and reverse *I-V* characteristics are highly temperature dependant. In the case of silicon carbide, the reverse leakage current increases by 4% /K, the reverse breakdown voltage decreases by -4% /K while a 0.45% /K increase in on-state voltage means die can be readily parallel connected, although non-repetitive current surge ability is decreased. In contrast, it will be noticed in figure 2.2 that reverse breakdown voltage and leakage current of a bipolar junction diode, both have a positive temperature co-efficient.

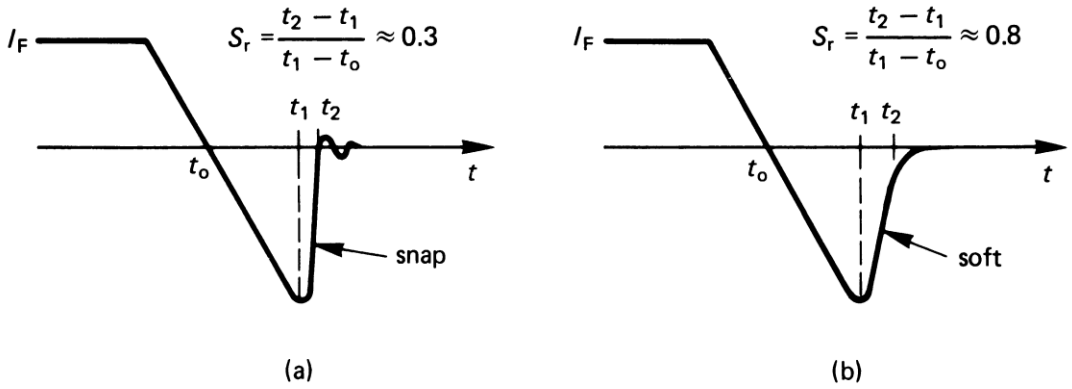

Figure 4.5. *Comparison of fast recovery diode di_{rr}/dt characteristics of:*
(a) short current tail, producing snap-off (low S_r) and
(b) gradual current tail, producing soft recovery (high S_r).

4.3 The bipolar, high-voltage, power switching npn junction transistor

The electrical properties of the high-voltage power switching npn transistor are related to and dominated by the wide low-concentration n^- collector region employed to obtain high-voltage characteristics in all semiconductor devices. Many of the limitations and constraints on the MOSFET, IGBT, and the different thyristors are due to their parasitic bjt structures, which introduce undesirable BJT characteristics and mechanisms. It is therefore essential to understand the electrical characteristics and properties of the BJT if the limitations of other switching semiconductor devices are to be appreciated.

4.3.1 Transistor ratings

4.3.1i – BJT collector voltage ratings

The breakdown voltage ratings of a transistor can be divided into those inherent to the actual transistor (V_{ceo}, V_{cbo}) and those that are highly dependent on the external base circuit conditions (V_{cer}, V_{ces}, V_{cev}).

Figure 4.6 shows the various voltage breakdown modes of the BJT, which are defined as follows.

V_{cbo} Collector to base voltage-current characteristics with the emitter open; that is, I_e = 0, where the voltage $V_{(BR)cbo}$ is the collector to base breakdown voltage with I_e = 0 and the collector current I_c specified as I_{cbo}.

V_{ceo} Collector to emitter characteristics with the base open circuit such that the base current I_b = 0, where $V_{(BR)ceo}$ is the collector to emitter breakdown voltage with I_b = 0 and I_c specified as I_{ceo}.

V_{ces} Collector to emitter characteristics with the base shorted to the emitter such that V_{be} = 0, where $V_{(BR)ces}$ is the collector to emitter breakdown voltage with I_c specified as I_{ces}.

V_{cer} Collector to emitter characteristics with resistance R between the base and the emitter such that R_{be} = R, where $V_{(BR)cer}$ is the collector to emitter breakdown voltage with I_c specified as I_{cer}.

V_{cev} Collector to emitter characteristics with reverse base to emitter bias V_{eb} = X, where $V_{(BR)cex}$ is the collector to emitter breakdown voltage with I_c specified as I_{cex}.

Each breakdown voltage level and its relative magnitude can be evaluated.

1 – BJT $V_{(BR)\text{cbo}}$ - maximum collector-base voltage with the emitter open circuit
The $V_{(BR)\text{cbo}}$ rating is just less than the voltage V_b, where the base to collector junction breaks down because of avalanche multiplication, as illustrated in figure 4.6. The common base avalanche breakdown voltage V_b is determined by the concentration of the collector n-region, N_c /cc, and as its resistivity increases, V_b increases according to (equation (2.3))

$$V_b = 5.34 \times 10^{13} \times N_c^{-3/4} \quad \text{(V)} \tag{4.7}$$

It can be assumed that $V_{(BR)\text{cbo}} \approx V_b$.

2 – BJT $V_{(BR)\text{ceo}}$ - maximum collector-emitter voltage with the base open circuit
Avalanche multiplication breakdown of a common emitter connected transistor occurs at a collector voltage V_a when the common emitter amplification factor β becomes infinite. The gain β, from equation (3.4) and accounting for avalanche multiplication, is defined by

$$\beta = \frac{\alpha_0 M}{1 - \alpha_0 M} \tag{4.8}$$

where M is the avalanche multiplication factor, which is collector junction voltage V_{cb} dependent, according to (equation (3.5))

$$M = 1 \Big/ \left(1 - \frac{V_{cb}}{V_b}\right)^m \tag{4.9}$$

The factor m is empirically determined and is between 2 and 4 for the collector-base doping profile of the high-voltage silicon npn transistor. The common base current amplification factor α_0 is for a voltage level well below any avalanche.

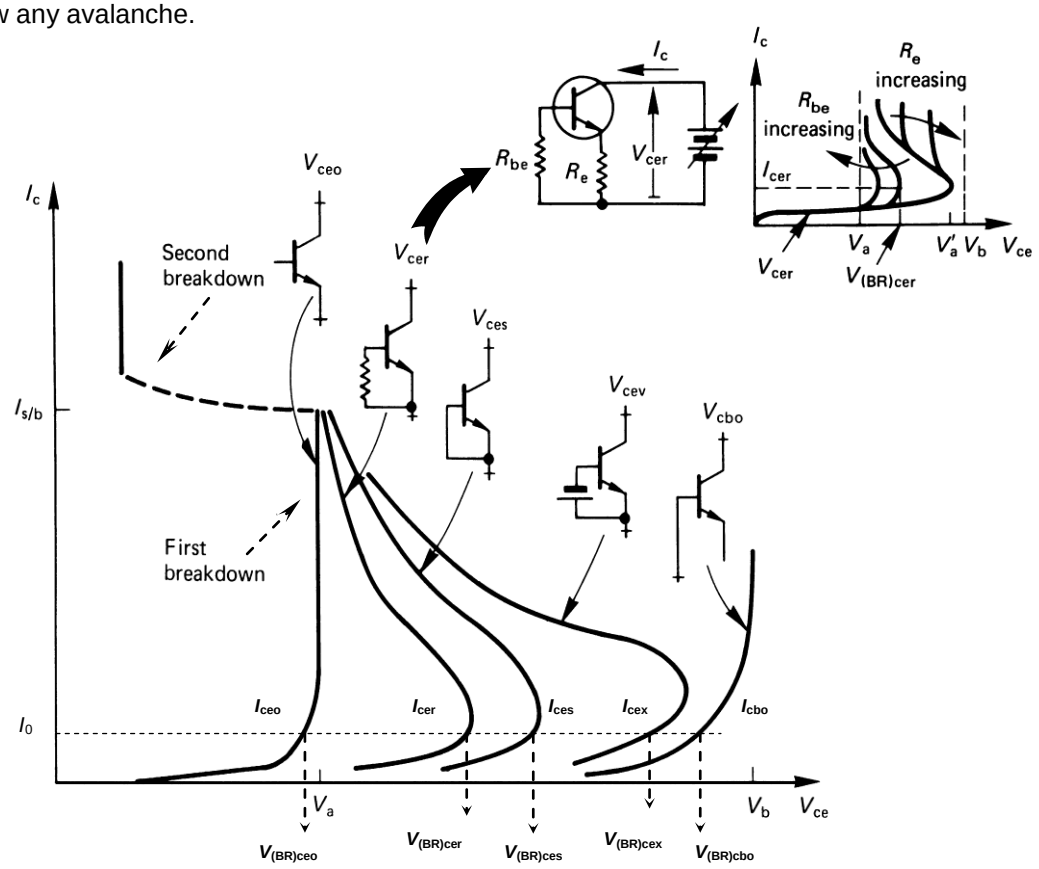

Figure 4.6. *Relative magnitudes of npn transistor collector voltage breakdown characteristics, showing first and second breakdown.*

At high V_{cb} voltages, near V_a, avalanche multiplication causes a high injection of hole carriers. Thus no base current is required and a $\beta \rightarrow \infty$ condition effectively occurs. With such conditions, equation (4.8) indicates that $\alpha_0 M \rightarrow 1$ which, upon substitution into equation (4.9), yields

$$V_a = V_b \sqrt[m]{1 - \alpha_0} \approx V_{(BR)\text{ceo}} \quad \text{(V)} \tag{4.10}$$

V_a becomes the common emitter avalanche breakdown voltage $V_{(BR)\text{ceo}}$ which is commonly called the collector emitter sustaining voltage, $V_{ceo(\text{sus})}$.

It can be shown that (see figure 4.6)

$$V_{(BR)\text{cbo}} > V_{(BR)\text{cex}} > V_{(BR)\text{ces}} > V_{(BR)\text{cer}} > V_{(BR)\text{ceo}} \tag{4.11}$$

With low-gain BJTs, V_a is almost V_b in value, but with high-gain devices V_b may be 2 to 3 times that of V_a. Notice in figure 4.6 that negative resistance characteristics occur after breakdown, as is the case with all the base circuit-dependent breakdown characteristics.

The inserted diagram in figure 4.6 shows how base-emitter resistance affects collector-emitter voltage breakdown. Importantly, the breakdown voltage increases as the base-emitter resistance decreases. This is because the injection efficiency of the emitter is reduced. This shorting feature is exploited extensively in alleviating parasitic problems in the MOSFET, IGBT, and thyristor devices, and is discussed in the respective device sections.

4.3.1ii – BJT safe operating area *(SOA)*

The safe operating area represents that electrical region where a transistor performs predictably and retains a high reliability, without causing device destruction or accelerated deterioration.

Deterioration or device destruction can occur when operating within the absolute maximum device ratings, as a result of second breakdown (s/b) or excessive thermal dissipation. Typical SOA characteristics are shown in figure 4.7. These collector characteristics are for a single pulse, of a given duration, such that the transistor operates in the linear region and at a case temperature of 25°C. The dc or continuous operation case has the most restrictive SOA curve, while a short single pulse of 1µs duration enables the full device *I*-*V* ratings to be exploited.

The SOA is basically bounded by the maximum collector $\hat{I}_c$ and the collector emitter breakdown voltage $V_{(BR)\text{ceo}}$. Figure 4.7 shows four distinct operating region limits, viz., A to D.

Ⓐ Maximum collector current which is related to allowed current density in the leads and contacts and the minimum gain of the transistor. The maximum lead current is given by $I = K_w d^{2/3}$ where the diameter d is in mm and K_w depends on the type and length of wire. For lengths greater than 1mm, K_w = 160 for both copper and silver.

Ⓑ Maximum thermal dissipation, which is related to the absolute maximum junction temperature $\hat{T}_j$, and the thermal resistance or impedance from the virtual junction to the case. In this thermally limited region, the collector power loss is constant and $I_c = PV_c^{-1}$. Thus the thermal limit gradient is -1, when plotted on logarithmic axes as in figure 4.7.

Ⓒ Limit of forward second breakdown (s/b). This breakdown occurs when the local current density is too high and a hot spot is created which causes thermal runaway. The physical causes of the high current concentration phenomenon are a fall in electrical potential or instability of lateral temperature distribution in the base area. These occur as a consequence of base-width concentration non-uniformity, a faulty junction or improper chip mounting. A typical s/b characteristic is shown in figure 4.6, and is characterised by a rapid drop in collector voltage to the low-impedance area after s/b. The s/b SOA limit can be modelled by $I_c = PV_c^{-1}$ where *n,* the gradient in figure 4.7, ranges from 1.5 to 4 depending on the fabrication processes and structures that have been employed. S/b, with a forward-biased base emitter is usually characterised by a short circuit at the emitter periphery, since this area is more forward-biased than central regions because of lateral base resistance effects. S/b, with a reverse-biased base-emitter junction, occurs in the central emitter region because of current focussing to that area as a result of the same lateral base resistance effects.

Ⓓ Maximum collector voltage under worst case conditions. In switching applications the $V_{(BR)\text{ceo}}$ limit can be exceeded provided suitable base conditions exist. At turn-off, when the collector current has fallen below I_{cex}, the collector supporting voltage can be increased from $V_{(BR)\text{ceo}}$ to $V_{(BR)\text{cex}}$ if the proper reverse bias base emitter junction conditions exist. The SOA together with this small extension area form the *reverse bias SOA.* Turn-on in switching applications can take place from a $V_{(BR)\text{cex}}$ condition, provided the collector current rise time is very short, usually much less than 1µs. As the rise time value decreases, the current that can be switched at turn-on increases. Under such conditions a significant portion of $\hat{I}_c$ can be switched from $V_{(BR)\text{cex}}$. The SOA together with this large switch-on extension area form the *forward bias SOA,* as shown in figure 4.7.

The SOA is usually characterised for a case temperature of 25°C. In practice much higher case temperatures are utilised and then the power and s/b SOA limits are modified with the aid of the derating curves of figure 4.8. At a given case temperature, above 25°C, power derating is greater than s/b derating. No derating is necessary for case temperatures below 25°C.

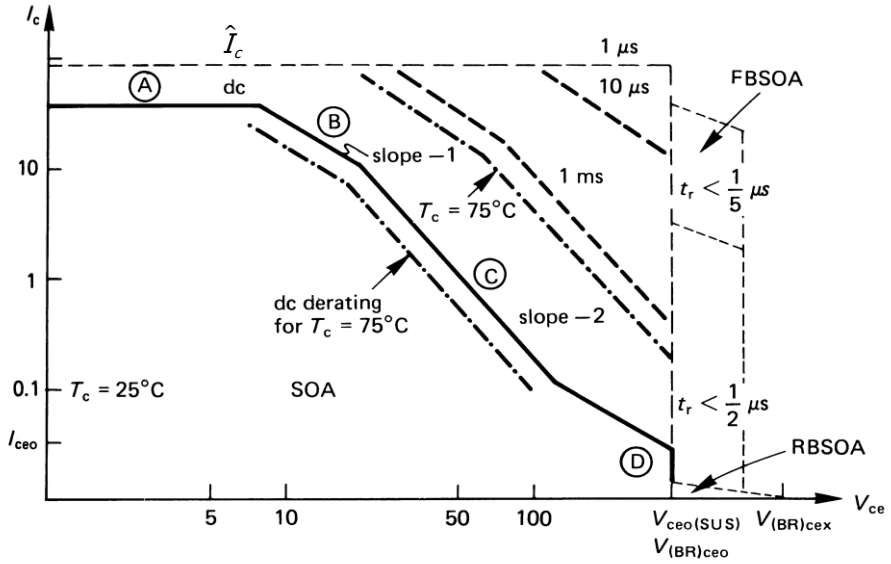

Figure 4.7. *Safe operating area (SOA) bounds of an npn high-voltage power switching transistor including forward and reverse bias SOA. Temperature derating for a case temperature of 75°C is shown.*

Figure 4.7 shows the derating, according to figure 4.8, of the dc and 1ms operating loci when the case temperature is increased from 25°C to 75°C. Figure 4.8 indicates that the power limit line is derated to 71.5 per cent, while the s/b limit line is reduced to 80 per cent. The slope of the 10μs single pulse limit line indicates that no s/b component exists, thus only power derating need be employed. This is because the pulse period of a few microseconds is short compared to the die thermal constant, whence the rate of local heating is too brief to disperse and cause second breakdown. But if the temperature rises, s/b effects will start to emerge into the characteristic locus.

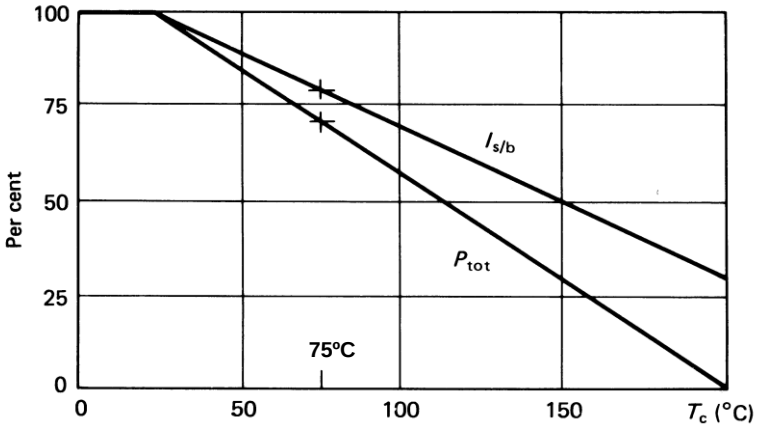

Figure 4.8. *Power and second breakdown derating versus case temperature.*

It is important to note that when a transistor is employed in a switching application, where the device is either cut-off or hard-on, the full SOA bounded by $\hat{I}_c$ and $V_{(BR)ceo}$ can usually be exploited. As indicated in figure 4.7, provided the collector switching times are of the order of a microsecond or less, no power or s/b derating need be factored. Design is based on total power losses, such that the maximum allowable junction temperature, $\hat{T}_j$ is not exceeded. For high reliability and long device lifetime only one electrical limit, either $\hat{I}_c$ or $V_{(BR)ceo}$, should be exploited in a given application.

4.3.2 Transistor switching characteristics

If a current pulse is supplied into the base of a common emitter connected transistor, as shown in figure 3.8, the resultant collector current waveform is as shown in figure 4.9. The collector voltage waveform is essentially collector load circuit dependent and therefore is not used to characterise transistor switching.

4.3.2i – BJT turn-on time: $t_{on} = t_d + t_{ri}$
Turn-on consists of a delay time t_d followed by a current rise time t_{ri}.
The delay time corresponds mainly to the charging of the base-emitter junction diffusion capacitance. The turn-on delay time can be significantly reduced by increasing the applied rate and magnitude of the forward base current I_{bf}.
The current rise time is related to the effective base zone width and, as the base charge increases because of the base current, the collector current increases.

4.3.2ii – BJT turn-off time: $t_{off} = t_s + t_{fi}$

In order to cut-off a transistor from the saturated state, all the accumulated charges must be neutralised or removed from the base and from the lightly doped n^- region of the collector. The turn-off process is started by removing the forward base current I_{bf}, and applying the reverse base current I_{br}. The excess minority carriers, namely holes, in the collector n^- region are progressively reduced in the process of providing the collector current. The excess minority carriers in the base are removed by the reverse base current. The reverse base current does not influence the collector n^- region recombination process. The period after the cessation of positive base current until the transistor enters the linear region is termed storage or *saturation time*, t_s. Generally, and undesirably, the larger the forward gain β_f, the greater the saturation time, t_s.

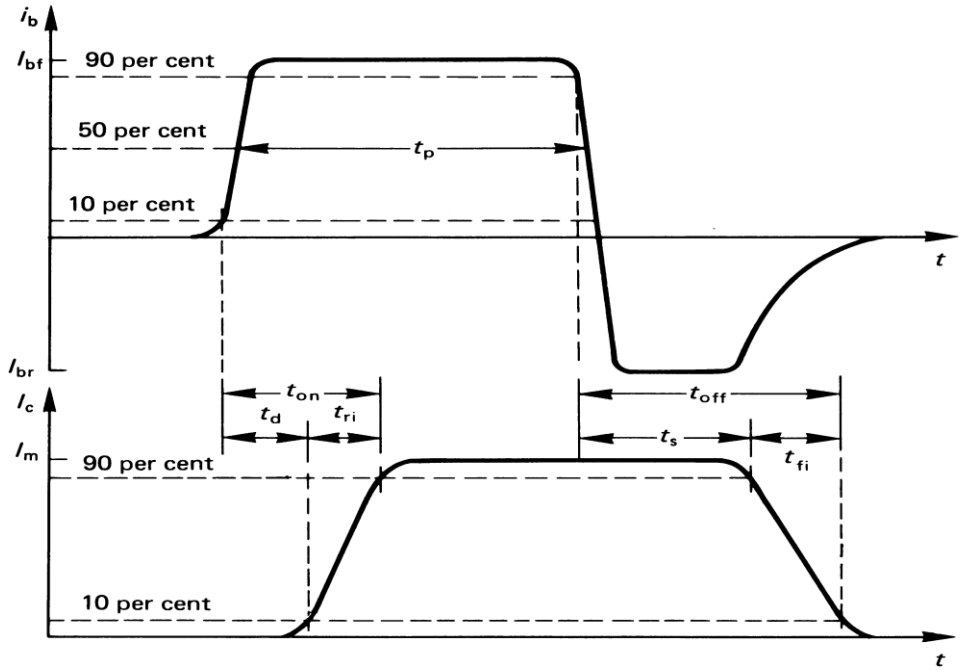

Figure 4.9. *Defining transistor base and collector current switching times for turn-on and turn-off.*

Optimal turn-off occurs when the emitter junction cuts off, as a result of I_{br}, just as the collector junction cuts off and enters the linear region. Thus the collector current fall time can be decreased by increasing the reverse base current immediately after the collector junction has cut off, which minimises the current fall time t_{fi}.

In switching applications, operation in the linear region is to be avoided, or at least traversed rapidly, because of the associated high device power losses. Although in the saturated state, with $I_{bf} >> I_c / \beta_f$, gives minimum forward gain and losses, this state is not conducive to a rapid turn-off transition to the cut-off region. In switching applications, in order to increase turn-off speed (decrease t_s and t_{fi}), the transistor may be held in the quasi-saturation region by reducing and controlling the forward base current magnitude such that the device is on the verge of saturation, $I_{bf} \approx I_c / \beta_f$, but is not in the linear region. The quasi-saturation on-state losses are slightly higher. In this state the collection n^- region can be considered as extra series collector circuit resistance, which decreases as the neutral base region penetrates and reduces to zero when saturation occurs.

4.3.3 BJT phenomena

Although the silicon BJT is virtually obsolete as a discrete power switching device for new circuit designs, it has been considered in some detail both in this chapter and chapter 3.2.1. This is because its operating electrical mechanisms explain the major limiting electrical operating factors of all controlled power switching devices.

- ***mosfet***: In chapter 3.2.2 the reverse conducting inherent body diode in the MOSFET is part of a parasitic npn transistor. This BJT structure can produce unwanted MOSFET *dv/dt* turn-on. Notice in figure 3.14a that the source metallization overlaps the p^+ well, there-in producing a base to emitter shunting resistor, as shown by R_{be} in figure 3.14b. The emitter shunts perform two essential functions, but inadvertently creates a non-optimal diode.
    - First, the shunt decreases the injection efficiency hence gain of the npn BJT, decreasing the likelihood of a drain *dv/dt* resulting in sufficient Miller capacitance current to turn-on the parasitic BJT, as considered in chapter 3.2.1.

- Second, by decreasing the BJT gain, the npn section voltage rating is increased from V_{ceo} to V_{cer} as considered in section 4.3.1.

- ***igbt***: In figure 3.16d the equivalent circuit of the IGBT has a parasitic pnp-npn thyristor structure. Once again, the emitter metallization (R_{be}) shunts the base to emitter of the npn BJT, helping to avoid latch-up of the SCR section, as modelled by the derivation of equation (3.25). Also the voltage rating of the npn section is increased from V_{ceo} to V_{cer}. Improved thermal stability also results. Judicious profiling of the transistor sections is essential.
- ***gto thyristor***: All the electrical operating mechanisms of the SCR are explainable in terms of BJT mechanisms, including turn-on, turn-off, and thermal stability. Emitter shorts (R_{be} shunts) are used extensively to decrease gain, increase thermal stability, and increase voltage ratings and are essential in providing separation in the bi-directional conducting thyristor, as considered in chapter 3.3.4. The GTO thyristor also uses emitter shorts in order to achieve a stable device at turn-off, as shown in figure 3.28.

An understanding of BJT electrical operating mechanisms is fundamental to the design and operation of semiconductor power switching devices, whether principally bipolar operating devices or unipolar devices which have bipolar parasitic structures.

4.4 The power MOSFET

The main electrical attributes offered by power MOSFETs are high switching speeds, no second breakdown (s/b), and high impedance on and off voltage control. MOSFETs, along with IGBTs, have replaced the bipolar junction transistor due to their superior switching performance and simpler gate control requirements.

4.4.1 MOSFET absolute maximum ratings

The basic enhancement mode power MOSFET structure and electrical circuit symbol are shown in figure 3.11. The SOA bounds shown in figure 4.10 is confined by four outer bounds.

(A) The n^- epitaxial layer concentration and thickness is the key parameter in specifying the drain high-voltage ratings, such as V_{ds} and V_{dg}, which increase with temperature at approximately +0.1 per cent/K, as shown in figure 3.13.

(B) One important rating feature of the power MOSFET is that it does not display the s/b that occurs with the bipolar transistor. Figure 4.10 shows the safe operating area for transistors, with the bipolar junction transistor s/b limitation area shaded. The physical explanation as to why MOSFETs do not suffer from s/b is based on the fact that carrier mobility in the channel decreases with increased temperature at -0.6 per cent/K. If localised heating occurs, the carrier mobility decreases in the region affected and, as a consequence, the localised current reduces. This negative feedback, self-protection mechanism forces currents to be uniformly distributed along the channel width and through the silicon die. This property is exploited when paralleling MOSFET devices. As a result of the enlarged SOA, the power MOSFET is generally a much more robust device than its bipolar counterpart. This region is thermally limited, as defined by $I = P/V^{-1}$ giving the -1 slope on the log-log axes in figure 4.10.

(C) The drain current rating is also related to the epitaxial properties. Its resistance specifies the $I_d^2 R_{ds(on)}$ power loss, which is limited by the junction to case thermal resistance, $R_{\theta\,\text{j-c}}$. The continuous, usable drain current above 25°C is thus given by

$$I_d = \sqrt{\frac{\hat{T}_j - T_c}{R_{ds(on)}\ R_{\theta\text{j-c}}}} \qquad \text{(A)} \qquad (4.12)$$

(D) When the MOSFET is on, with minimum drain voltage at maximum drain current, it operates in the resistive mode where the drain current is given by

$$I_d = \frac{1}{R_{ds(on)}} V_{ds} \qquad \text{(A)} \qquad (4.13)$$

The SOA region at high currents and low voltages is thus characterised by a line of slope 1, on logarithmic axes, as shown in figure 4.10.

The gate to source voltage V_{gs} controls the channel and the higher the value of V_{gs}, the higher the possible drain current. The gate to source is a silicon dioxide dielectric capacitor which has an absolute forward and reverse voltage that can be impressed before dielectric breakdown. Typical absolute maximum voltage levels vary from ±10V to ±40V, as the oxide layer thickness increases and capacitance advantageously decreases.

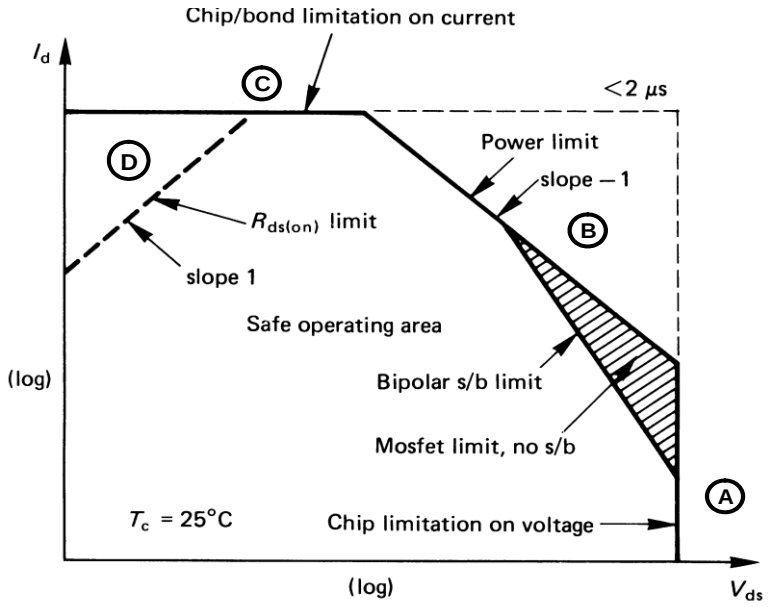

Figure 4.10. *The safe operating area of the power MOSFET, which does not suffer second breakdown.*

4.4.2 Dynamic characteristics

The important power MOSFET dynamic characteristics are inter-terminal voltage-dependent capacitance and drain current-switching times. The various MOSFET capacitances are dominant in specifying switching times.

4.4.2i – MOSFET device capacitances

Figure 4.11 shows an equivalent circuit for the power MOSFET, extracted from figure 3.14, which includes three inter-terminal, non-linear voltage-dependent capacitances C_{gd}, C_{gs}, and C_{ds}. The magnitudes are largely determined by the size of the chip and the cell topology used. Therefore higher current devices, with a given voltage rating, inherently have larger capacitances. Electrically, these capacitances are strongly dependent on the terminal drain-source voltage.

Manufacturers do not generally specify C_{gd}, C_{gs}, and C_{ds} directly but present input capacitance C_{iss}, common source output capacitance C_{oss}, and reverse transfer capacitance C_{rss}. These capacitances, as a function of drain to source voltage, are shown in figure 4.12a. The manufacturers' quoted capacitances and the device capacitances shown in figure 4.12b are related according to

$$C_{iss} = C_{gs} + C_{gd}; \qquad C_{ds} \text{ shorted} \qquad \text{(F)} \tag{4.14}$$

$$C_{rss} = C_{gd} \qquad \text{(F)} \tag{4.15}$$

$$C_{oss} = C_{ds} + \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}}; \qquad C_{gs} \text{ shorted} \qquad \approx C_{ds} + C_{gd} \qquad \text{(F)} \tag{4.16}$$

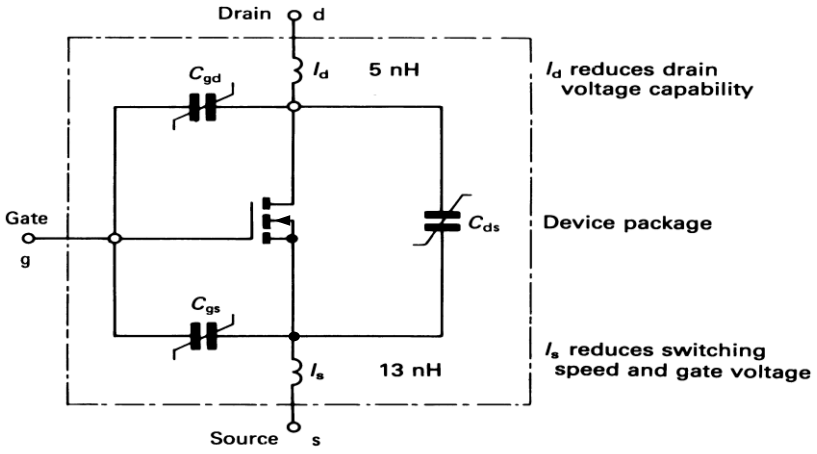

Figure 4.11. *MOSFET equivalent circuit including terminal voltage dependent capacitance and inductance for the TO247 package.*

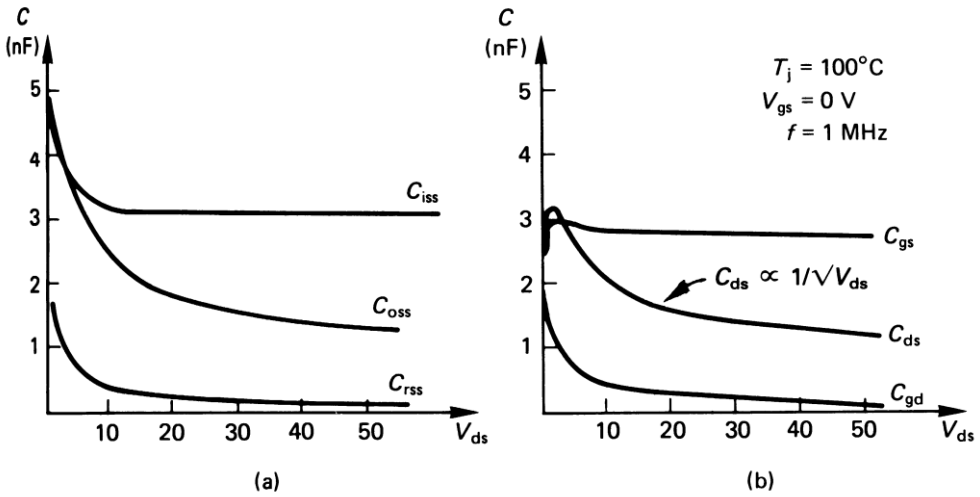

Figure 4.12. *MOSFET capacitance variation with drain-to-source voltage: (a) manufacturers' measurements and (b) inter-terminal capacitance values.*

The measurement frequency is usually 1 MHz and any terminals to be shorted are connected with large, high-frequency capacitance, so as to present a short circuit at the measurement frequency.

Device capacitances are predominant in specifying the drain current switching characteristics, particularly C_{gd} with its large capacitance variation at low drain voltage levels.

4.4.2ii – MOSFET switching characteristics

The simple single-ended MOSFET circuit with an inductive load L_L in figure 4.13, can illustrate how device capacitances influence switching. The MOSFET gate is driven from a voltage source whose output impedance is represented by R_g, which also includes any MOSFET gate series internal resistance. The dc input resistance of a power MOSFET is in excess of 10^{12} Ohms and when used as a switch, the power required to keep it on or off is negligible. However energy is required to change it from the off state to the on state, as shown in figure 4.14. This figure shows the relationship between gate charge, gate voltage, and drain current for a typical MOSFET. The initial charge Q_{gs} is that required to charge the gate-source capacitance and Q_{gd} is that required to supply the drain-gate Miller capacitance. For a given gate charging current, switching speed is proportional to gate voltage. The gate charge required for switching, and hence switching speed, is not influenced significantly by the drain current magnitude, and not at all by the operating temperature. The switching speed is directly related to time delays in the structure because of the channel transit time of electrons. External to the device, the switching time is determined by the energy available from the drive circuit. A gate drive design example based on gate charge requirement is presented in chapter 8.1.2.

The switching transients can be predicted for an inductive load, when the load is the parallel inductor and diode, with no stray unclamped inductance, as shown in figure 4.13. It is assumed that a steady load current I_L flows. The various turn-on and turn-off periods shown in figure 4.15 are related to the sequential charging periods shown in figure 4.14. Any gate circuit inductance is neglected.

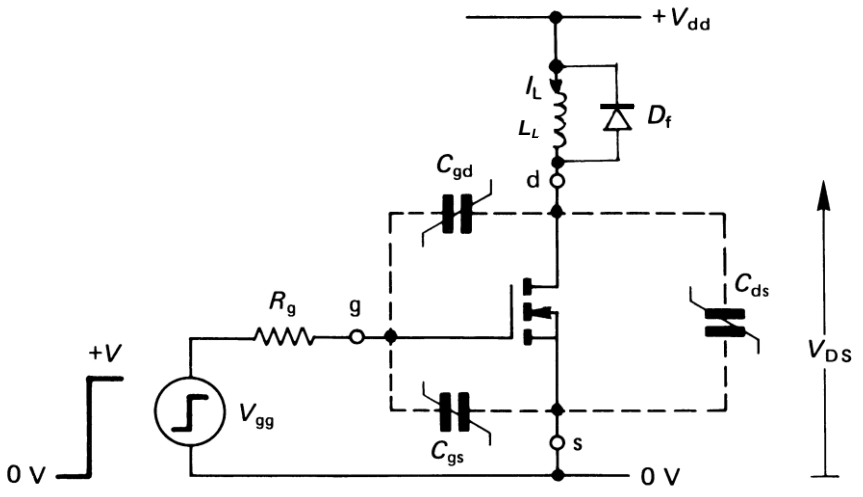

Figure 4.13. *MOSFET basic switching circuit used to demonstrate current switching characteristics.*

***1 – MOSFET** turn-on*

Period I - turn-on delay, $t_{d\,on}$

The gate voltage rises exponentially to the gate threshold voltage V_{TH} according to equation (4.17), that is

$$V_{gs}(t) = V_{gg}\,[1 - e^{-t/C_{in}R_g}] \qquad \text{(V)} \qquad (4.17)$$

where C_{in}, the gate input capacitance is approximated by $C_{gd} + C_{gs}$, or C_{iss}. The drain voltage remains unchanged, that is, it supports the supply voltage V_{dd} and virtually no MOSFET drain current flows. The turn-on delay time is given by

$$t_{d\,on} = C_{in}R_g\ \ell n\left(1 - \frac{V_{Th}}{V_{gg}}\right)^{-1} \qquad \text{(s)} \qquad (4.18)$$

Equations (4.17) and (4.18) can be modified to account for a negative initial gate voltage (as presented in Appendix 4.8), a condition which increases the turn-on delay time, but increases input noise immunity.

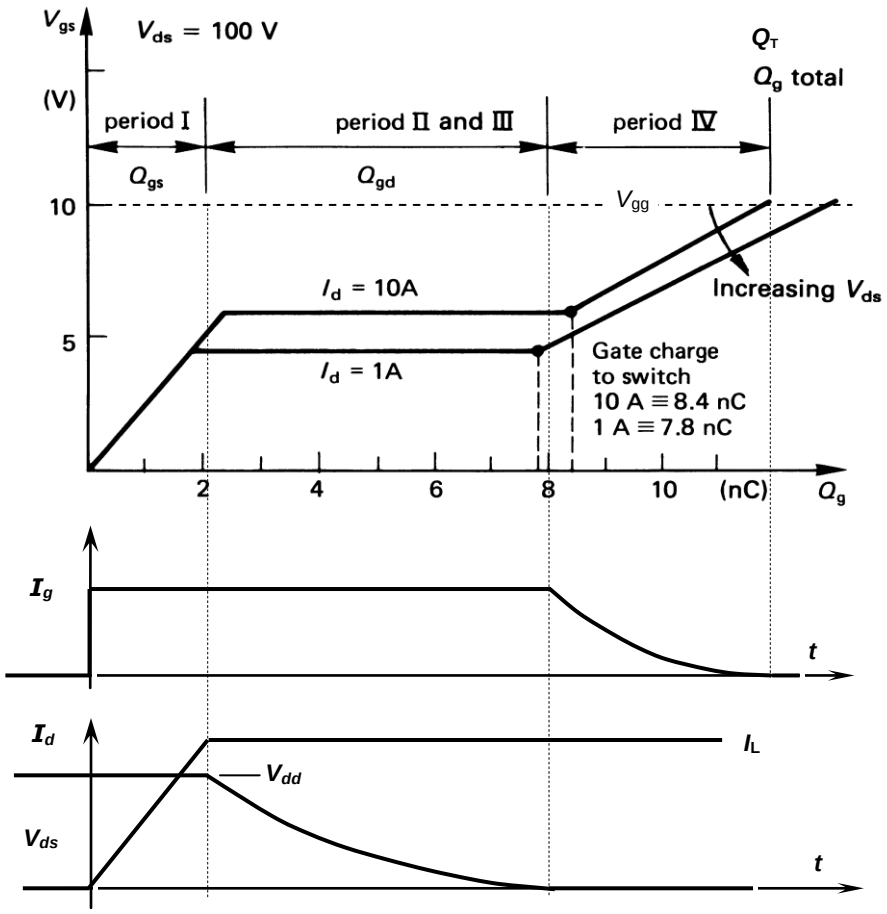

Figure 4.14. *Typical relationships between gate charge, voltage, and current and magnitude of drain current and voltage being switched.*

Period II - current rise, t_{ri}

Drain current commences to flow in proportion to the gate voltage as indicated by the transconductance characteristics in figure 3.12a. The gate voltage continues to rise according to equation (4.17). The drain voltage is clamped to the rail voltage V_{dd} and the drain current rises exponentially to the load current level I_L, according to

$$I_d(t) = g_{fs}\,(V_{gg} - V_{Th})\,[1 - e^{-t/R_gC_{in}}] \qquad \text{(A)} \qquad (4.19)$$

The current rise time t_{ri} can be found by equating $I_d = I_L$ in equation (4.19).

$$t_{ri} = R_gC_{in}\ell n\left(\frac{g_{fs}(V_{gg} - V_{Th})}{g_{fs}(V_{gg} - V_{Th}) - I_L}\right) \qquad (4.20)$$

Period III - voltage fall, t_{fv}

When the drain current reaches the load current level, the drain voltage will fall from V_{dd} to the low on-state voltage. This decreasing drain voltage produces a feedback current via C_{gd} to the gate, which must be provided by the gate drive. This feedback mechanism is called the *Miller effect* and the effective gate input

capacitance increases to $C_{in} = C_{iss} + (1 - A_v)C_{gd}$ where $A_v = \Delta V_{ds} / \Delta V_{gs}$. For a constant load current, from figure 3.12a, the gate voltage remains constant at

$$V_{gs} = V_{Th} + I_L / g_{fs} \quad \text{(V)} \tag{4.21}$$

as shown in figure 4.15b.
Since the gate voltage is constant, the Miller capacitance C_{gd} is charged by the constant gate current

$$I_g = \frac{V_{gg} - V_{gs}}{R_g} = \frac{V_{gg} - (V_{Th} + I_L / g_{fs})}{R_g} \quad \text{(A)} \tag{4.22}$$

and the rate of change of drain voltage will be given by

$$\frac{dV_{gd}}{dt} = \frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}} \quad \text{(V/s)} \tag{4.23}$$

that is

$$V_{ds}(t) = V_{dd} - \frac{I_g}{C_{gd}} t \quad \text{(V)} \tag{4.24}$$

The drain voltage decreases linearly in time and the voltage fall time is decreased by increasing the gate current. Assuming a low on-state voltage, the voltage fall time t_{fv} is given by

$$t_{fv} = V_{dd} C_{gd} / I_g = V_{dd} C_{gd} R_g / (V_{gg} - V_{Th}) \quad \text{(s)} \tag{4.25}$$

Period IV
Once the drain voltage reaches the low on-state voltage, the MOSFET is fully on and the gate voltage increases exponentially towards V_{gg}.

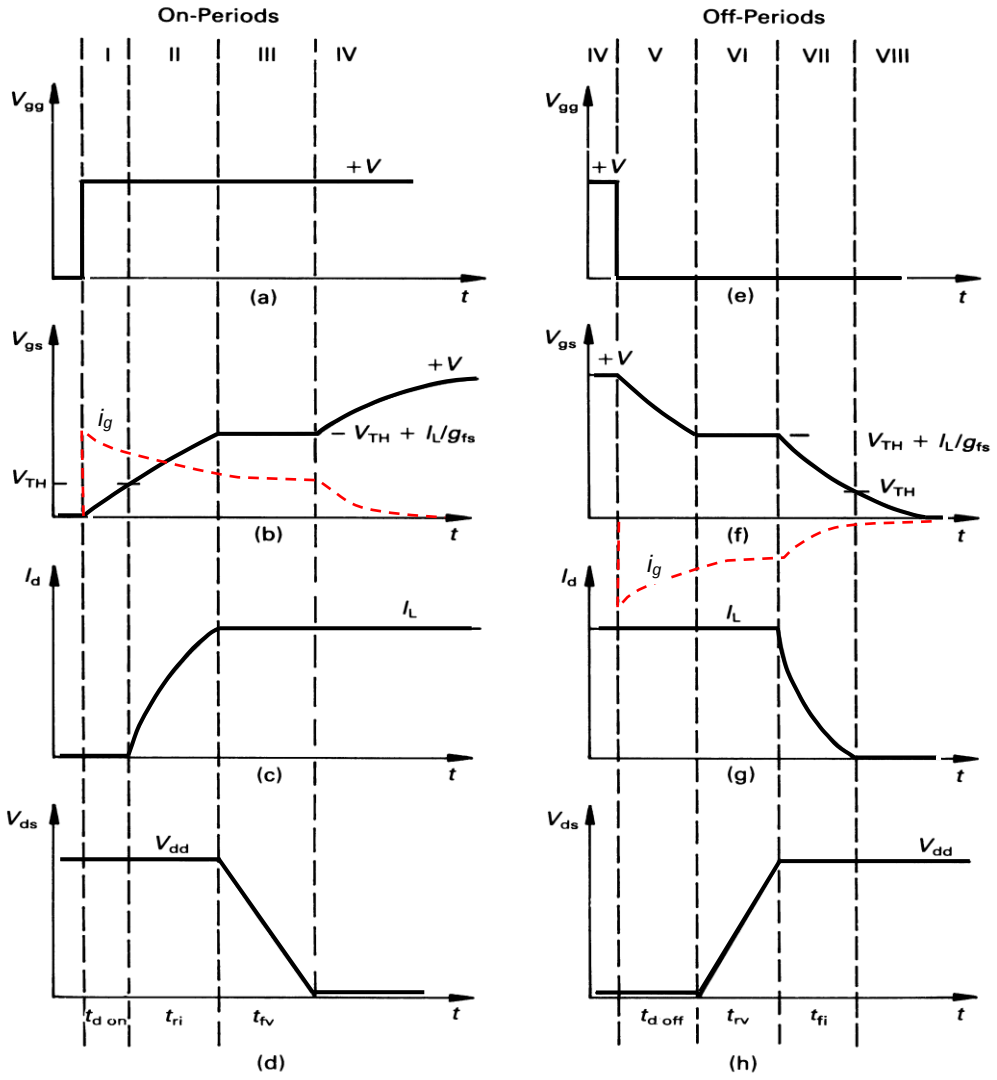

Figure 4.15. *Distinct switching periods of the MOSFET with an inductive load at: (a) (b) (c) (d) comprising turn-on; (e) (f) (g) (h) forming turn-off.*

***2 – MOSFET** turn-off*

Period V - turn-off delay, $t_{d\,off}$
The MOSFET is fully on, conducting the load current I_L, and the gate is charged to V_{gg}. The gate voltage falls exponentially from V_{gg} to $V_{Th} + I_L/g_{fs}$ according to

$$V_{gs}(t) = V_{gg}\, e^{-t/R_g C_{in}} \quad \text{(V)} \qquad (4.26)$$

in a time given by

$$t_{d\,off} = R_g C_{in}\, \ell n \frac{V_{gg}}{V_{Th} + I_L / g_{fs}} \quad \text{(s)} \qquad (4.27)$$

This delay time can be decreased if a negative off-state gate bias is used. The drain conditions are unchanged.

Period VI - voltage rise, t_{rv}
The drain voltage rises while the drain current is fixed to the load current level, I_L. Accordingly the gate voltage remains constant and the gate current is given by

$$I_g = \frac{V_{Th} + I_L / g_{fs}}{R_g} \quad \text{(A)} \qquad (4.28)$$

This current discharges the Miller capacitance according to

$$\frac{dV_{ds}}{dt} = \frac{dV_{dg}}{dt} = \frac{I_g}{C_{gd}} \quad \text{(V/s)} \qquad (4.29)$$

Thus $$V_{ds}(t) = \frac{I_g}{C_{gd}}\, t \quad \text{(V)} \qquad (4.30)$$

where the low on-state voltage has been neglected.
The voltage rise time t_{rv} is given by

$$t_{rv} = \frac{C_{gd}\, V_{dd}}{I_g} \quad \text{(s)} \qquad (4.31)$$

and is decreased by increasing the gate reverse current magnitude. The drain voltage rises linearly to the dc supply V_{dd}.

Period VII - current fall, t_{fi}
When the drain voltage reaches the supply rail, the load current in the MOSFET begins to decrease, with load current being diverted to the diode D_f.
The gate voltage decreases exponentially according to

$$V_{gs}(t) = (V_{Th} + I_L / g_{fs})\, e^{-t/R_g C_{in}} \quad \text{(V)} \qquad (4.32)$$

and is mirrored by the drain current

$$I_d(t) = (I_L + g_{fs} V_{Th})\, e^{-t/R_g C_{in}} - g_{fs} V_{Th} \quad \text{(A)} \qquad (4.33)$$

The current fall time t_{fi} is given by $I_d = 0$ in equation (4.33) or when the gate-source voltage reaches the threshold voltage, that is, from equation (4.32)

$$t_{fi} = R_g\, C_{in} \ell n \left(1 + \frac{I_L}{g_{fs}\, V_{Th}}\right) \quad \text{(s)} \qquad (4.34)$$

Period VIII – off-state
The MOSFET drain is cut-off and the gate voltage decays exponentially to zero volts according to

$$V_{gs}(t) = V_{Th}\, e^{-t/R_g C_{in}} \quad \text{(V)} \qquad (4.35)$$

Based on the total gate charge Q_T delivered by the gate source V_{gg}, shown in figure 4.14, the power dissipated in the MOSFET internal gate resistance, hence contributing to device losses, is given by

$$P_G(R_{int}) = V_{gg} Q_T f_s \frac{R_{g\,int}}{R_{g\,int} + R_{g\,ext}} \quad \text{(W)} \qquad (4.36)$$

Example 4.1: ***MOSFET drain characteristics***

A power mosfet with
C_{gs}=1nF, C_{gd}=200pF, g_{fs}=4 and the threshold voltage is 3V,
is used to switch a 200V dc 20A load. If the gate is sourced from a 15V voltage source via a 10Ω gate resistance, what is the maximum rate of rise of drain current and voltage?

Solution

From equation (4.21), during turn-on:

$$i_D = g_{fs}\left(V_{gs} - V_{Th}\right)$$

whence

$$\frac{di_D}{dt} = g_{fs}\frac{dV_{gs}}{dt}$$

From equation 4.23

$$\left(C_{gs} + C_{gd}\right)\frac{dV_{gs}}{dt} = I_g = \frac{V_{gg} - V_{gs}}{R_g}$$

Combining these equations

$$\frac{di_D}{dt} = g_{fs}\frac{dV_{gs}}{dt} = g_{fs}\frac{I_g}{\left(C_{gs} + C_{gd}\right)} = g_{fs}\frac{V_{gg} - V_{gs}}{\left(C_{gs} + C_{gd}\right)R_g}$$

The maximum drain di/dt occurs at the gate threshold voltage, that is

$$\left|\frac{di_D}{dt}\right|_{\max} = \frac{g_{fs}}{\left(C_{gs} + C_{gd}\right)}I_g^{\max} = \frac{g_{fs}}{\left(C_{gs} + C_{gd}\right)R_g}\left(V_{gg} - V_{gs}^{\min}\right)$$

$$= \frac{g_{fs}}{\left(C_{gs} + C_{gd}\right)R_g}\left(V_{gg} - V_{Th}\right)$$

$$= \frac{4}{\left(1\text{nF} + 200\text{pF}\right)\times 10\Omega}\left(15\text{V} - 3\text{V}\right) = 4\text{kA/}\mu\text{s}$$

From equation (4.23)

$$\frac{dV_{gd}}{dt} = \frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}} = \frac{V_{gg} - V_{gs}}{C_{gd}R_g} \qquad \text{(V/s)}$$

The maximum drain *dv/dt* occurs at the gate threshold voltage, that is

$$\left|\frac{dV_{ds}}{dt}\right|_{\max} = \frac{I_g^{\max}}{C_{gd}} = \frac{V_{gg} - V_{gs}^{\min}}{C_{gd}R_g}$$

$$= \frac{V_{gg} - V_{Th}}{C_{gd}R_g}$$

$$= \frac{15\text{V} - 3\text{V}}{200\text{pF}\times 10\Omega} = 6\text{kV/}\mu\text{s}$$

♣

4.5 The insulated gate bipolar transistor

4.5.1 IGBT switching

The IGBT gate charge characteristics for switching and the switching waveforms are similar to those of the MOSFET, shown in figures 4.14 and 4.15 respectively, whilst the *I-V* on and off state characteristics are similar to the BJT. The collector switching characteristics depend on the injection efficiency of the collector p^+ emitting junction. The higher the injection efficiency, the higher the pnp transistor section gain and the lower the on-state voltage. The poorer the injection efficiency, the more the characteristics resemble a MOSFET.

The turn-on waveforms and mechanisms are essentially those for the MOSFET shown in figure 4.15. Figure 4.16 shows IGBT turn-off which has components due to MOSFET and BJT action. As with the MOSFET, distinct turn-off stages exist when switching an inductive load.

Period V - turn-off delay, $t_{d\,\text{off}}$

The gate voltage falls to a level determined by the gate threshold, V_{TH}, the forward transconductance, g_{fs} and the MOSFET section current level.

Period VI - voltage rise, t_{rv}

As the collector voltage rises the collector current remains constant, hence the gate voltage remains constant while charging the Miller capacitance. For a high gain pnp section the voltage rise time is virtually independent of gate resistance, while for an IGBT closely resembling a MOSFET the voltage rise is gate current magnitude dependent.

Period VII - current fall, t_{fi}
The current falls in two stages, the first, phase VII, due to MOSFET action, as are the previous two phases (periods V and VI). As with the conventional MOSFET the current falls rapidly as the MOSFET section current, shown in figure 4.16b reduces to zero.

Period VIII – current tail time
With the gate voltage at the threshold level, the pnp transistor section turns off in a V_{ceo} mode, phase VIII. A relatively low-magnitude, lengthy current tail results which is dependent on the pnp transistor section minority carrier lifetime in the n base and the injection efficiency of the p^+ collector region.

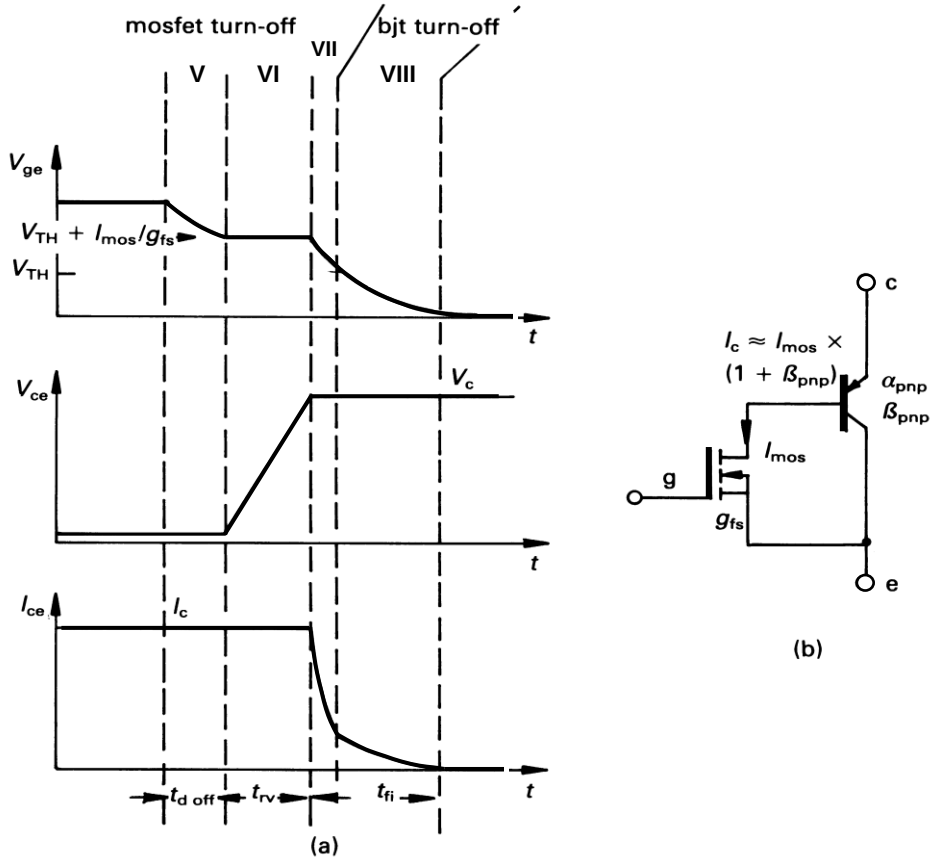

Figure 4.16. *IGBT: (a) turn-off waveforms and (b) equivalent circuit during turn-off.*

The switching frequency and current rating of an IGBT are both limited by the minimum of the package dissipation limit (as with any other semiconductor device) and a factor solely dependant on the switching times at turn-on and turn-off. As the switching frequency increases, the current rating decreases. Unlike the IGBT, the MOSFET upper frequency is restricted solely by losses, that is, temperature.

4.5.2 IGBT short circuit operation

Under certain electrical conditions the IGBT may be subjected to short circuits, and safely turned off without deterioration or damage. Two different short circuit conditions are characterised:

- **i.** IGBT turn-on into a pre-existing load short circuit, or *hard switch fault*.
- **ii.** Subsequent to IGBT turn-on, a short circuit load condition occurs during the on-state period, or *fault under load*.

i. Pre-existing short circuit at turn-on
The collector electrical characteristics are determined by the gate drive parameters and conditions. As the collector voltage falls, the collector current *di/dt* is determined by the stray inductance, characterised at less than 25µH. In this fault mode the IGBT is characterised for up to ten times the rated current, provided the IGBT is turned off within 10us, but at a slower rate than normal.

ii. Short circuit arising during the normal on-period

When a load short circuit occurs during the IGBT on period, the collector current rises rapidly and is determined by the supply voltage V_s and stray inductance L_s according to $di_{rise}/dt = V_s/L_s$. The collector voltage de-saturates and as the collector voltage rises towards the supply V_s the resultant dv/dt produces a Miller capacitance charging current, which flows into the gate circuit. Depending on the gate drive impedance, the gate voltage rises, which adversely allows higher collector current.
When turn-off is initiated, by reducing the gate voltage to below the threshold level, the resultant collector current fall produces a high voltage across the stray inductance, $V_{Ls} = L_s\ di_{fall}/dt$, which adds to the collector voltage which is already near the supply rail V_s. Because of this over voltage, this mode of short circuit turn-off is more severe than turning off from a pre-existing short circuit.
The maximum allowable short circuit current at turn-off is dependant on the gate voltage and reduces from ten times rated current at a gate voltage of 18V down to five times rated current at 12V. The short circuit must be commutated within 10us at a slower than normal rate so as to ensure the over voltage due to stray inductance remains within rated voltage limits. Repetitive short circuits are restricted to a frequency of less than one Hertz and can only accumulate to 1000 before device deterioration accelerates; both mechanical bonding and electrical.

Stress during the fault period can be reduced if the gate voltage is clamped so that it cannot rise during the Miller capacitance charge period. A Zener diode (plus a reverse series diode if reverse gate bias is used) across the gate to emitter provides low inductance gate voltage clamping, but the Zener standby to clamping voltage ratio of 1:1.4 limits clamping effectiveness. The preferred method is to clamp the gate to the gate supply voltage by a Schottky diode between the gate (diode anode) and gate positive supply (diode cathode). Judicious gate supply ceramic capacitance decoupling will minimise loop inductance which otherwise would deteriorate clamping effectiveness.
A difficulty arises when attempting to utilise the 10µs short circuit capabilities of the IGBT. To improve device robustness, short circuit turn-off is staged, or slowed down. It is prudent to utilise the over current capability of the IGBT in order to reduce nuisance tripping or to briefly ignore capacitor charging which are not true faults. A difficulty arises when a demand pulse is significantly less than 10µs. The gate drive must be able to cater for sub 10µs pulses with normal turn-off yet differentiate 10µs delayed slow turn-off when a short circuit fault is serviced.

Table 4.1: The IGBT Characteristics Comparison with the BJT and MOSFET

Features	BJT	MOSFET	IGBT
Drive Method	Current	Voltage	Voltage
Drive Circuit	Complex	Simple	Simple
Input Impedance	Low	High	High
Drive Power	High	Low	Low
Switching Speed	Slow (µs)	Fast (ns)	Middle
S.O.A.	Narrow	Wide	Wide
Saturation Voltage	Low	High	Low
Series Avalanche Operation	Excellent	Poor	Poor

4.6 The thyristor

Most of the thyristor ratings and characteristics to be considered are not specific to only the silicon-controlled rectifier, although the dynamic characteristics of the gate turn-off thyristor are considered separately.

4.6.1 SCR ratings

The fundamental four layer, three junction thyristor structures and their basic electrical properties were considered in chapter 3.3.

4.6.1i - SCR anode ratings

Thyristors for low-frequency application, such as in 50-60 Hz and 300-360 Hz, 400Hz ac supply systems, are termed *converter-grade* thyristors. When a higher switching frequency is required, so-called *gate commutated* devices like the GTO and GCT are applicable. Such devices sacrifice voltage and current ratings for improved self-commutating capability.

The repetitive peak thyristor voltage rating is that voltage which the device will safely withstand in both the forward off-state V_{DRM}, and reverse direction V_{RRM}, without breakdown. The voltage rating is primarily related to reverse leakage or forward blocking current I_{RRM} and I_{DRM} respectively, at a given junction temperature, usually 125°C. Since forward blocking current doubles with every 10K rise in junction temperature T_j, power dissipation increases rapidly with T_j, which may lead to regenerative thermal runaway, turning the device on in the forward direction.

Current related maximum ratings reflecting application requirements include

- peak one cycle surge on-state current I_{TSM}
- repetitive and non-repetitive *di/dt*
- I^2t for fusing.

The maximum junction temperature can be exceeded during non-recurrent over-current cycles. The maximum non-repetitive on-state surge current is generally quoted for one 10 millisecond sinusoidal period at $\hat{T}_j$. Any non-recurrent rating can be tolerated only a limited number of times before failure results. Such non-recurrent ratings are usually specified to allow fuse and circuit breaker short-circuit protection. The I^2t rating for a 10ms period is another parameter used for fuse protection, where I is non-repetitive rms current. When used in 60Hz systems the ratings are specified with respect to 8.33ms.

If the device is turned on into a fault, the initial current-time relationship, *di/dt*, during turn-on must be within the device's switching capability. In cases where the initial *di/dt* is rapid compared with the active plasma area-spreading velocity of 50 µm/µs, local hot spot heating will occur because of the high current densities in those areas that have started to conduct.

A repetitive *di/dt* rating is also given for normal operating conditions, which will not lead to device deterioration. This repetitive *di/dt* rating will be specified for a given initial blocking voltage and peak forward current. Certain gate drive conditions are specified and the device must survive for 1000 hours.

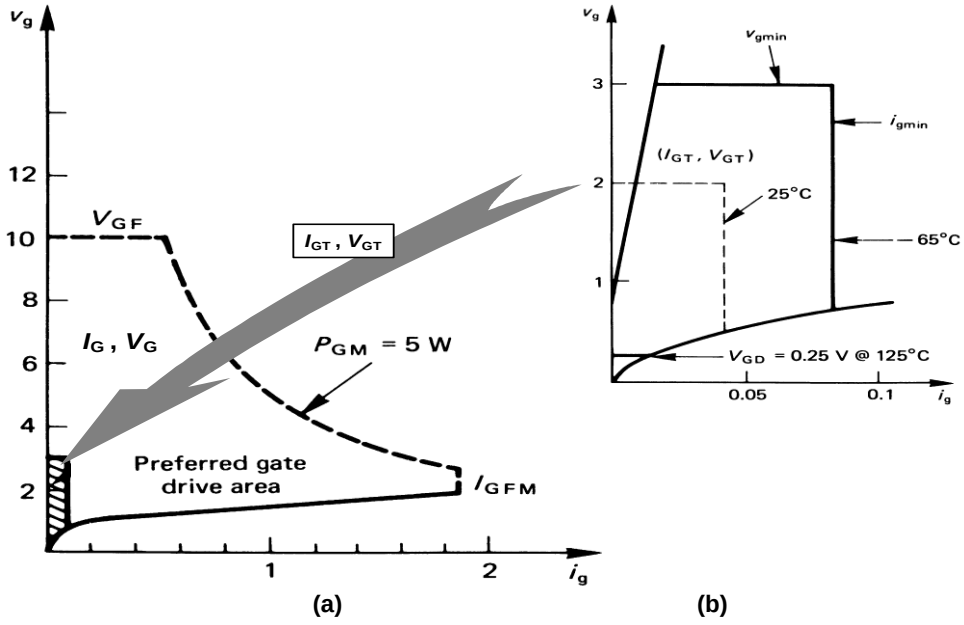

Figure 4.17. *Thyristor gate ratings illustrating: (a) the preferred operating region and (b) minimum gate requirements and their temperature dependence.*

4.6.1ii - SCR gate ratings

The gate ratings usually specified are

- peak and mean gate power, P_{GM} and P_G
- peak forward and reverse gate to cathode voltage, V_{GFM} and V_{GRM}
- peak forward gate current, I_{FMG}.

These gate ratings are illustrated in figure 4.17. The peak gate power rating is obtained by using a low duty cycle pulse, with a mean power that does not exceed P_G. The reverse gate voltage limit, V_{GRM}, is specified by the avalanche voltage breakdown limit of the reverse-biased gate-to-cathode junction. Figure 4.17 not only shows limit ratings, it also indicates the preferred gate voltage and current, and the minimum requirements which will ensure turn-on at different junction temperatures.

4.6.2 Static characteristics

The static anode voltage-current characteristics of a thyristor are similar to those of a diode. Gate commutated thyristors tend to have higher on-state voltages for a given current than comparable converter-grade devices. This higher on-state voltage is one of the trade-offs in improving the switching performance.

4.6.2i - SCR gate trigger requirements

Below a certain gate voltage, called the *gate non-trigger voltage* V_{GD}, the manufacturer guarantees that no device will trigger. This voltage level is shown in figure 4.17b. The hatched insert area in figure 4.17a (figure 4.17b) contains all the possible minimum trigger values (I_{GT}, V_{GT}) for different temperatures, that will result in turn-on. The gate requirements (I_{GT}, V_{GT}) have a negative temperature coefficient as indicated in figure 4.17b. To ensure reliable turn-on of all devices, independent of temperature, the trigger circuit must provide a dc signal (I_G, V_G) outside the shaded area. This area outside the uncertainty area, but within the rating bounds, is termed the *preferred gate drive* area.

An increase in anode supporting voltage tends to decrease the gate drive requirements. But if the gate signal is a pulse of less than about 100µs, the turn-on *(*I_G, V_G) requirement is increased as the pulse duration is decreased. The gate current increase is more significant than the voltage requirement increase. Typically, for a pulse reduced from 100µs to 1µs, the voltage to current increase above the original requirement is 2:10 respectively. This increased drive requirement with reduced pulse time is accounted for by the fact that some of the initial gate p-region charge recombines. When the free charge reaches a certain level the device triggers. Thus, to get the required charge into the gate in a relatively short time compared with the recombination time requires higher current, and hence higher voltage, than for dc triggering.

4.6.2ii – SCR holding and latching currents

If the on-state anode current drops below a minimum level, designated as the *holding current* I_H, the thyristor reverts to the forward blocking state. This occurs because the loop gain of the equivalent circuit pnp-npn transistors falls below unity and the regenerative hold-on action ceases. The holding current has a negative temperature coefficient; that is, as the junction temperature falls, the device holding current requirement increases. The holding current is typically about 2% of the rated anode current, and increases as switching performance is improved (and on-state voltage increases).

A somewhat higher value of anode on-state current than the holding current is required for the thyristor to latch on initially ($I_L > I_H$). If this higher value of anode *latching current* I_L is not reached, the thyristor will revert to the blocking state as soon as the gate trigger signal is removed. After latch-on, however, the anode current may be reduced to the holding current level, without turn-off occurring. These two static current properties are shown in the *I-V* characteristics in figure 3.22. With inductive anode circuits, it is important to ensure that the anode current has risen to the latching current level before the gate turn-on signal is removed. Continuous gate drive avoids this inductive load problem but at the expense of increased thyristor gate power losses.

4.6.3 Dynamic characteristics

The main thyristor dynamic characteristics are the turn-on and turn-off switching intervals, which are associated with the anode and gate circuit interaction.

4.6.3i – SCR anode at turn-on

Turn-on comprises a delay time t_d and a voltage fall time t_{fv}, such that the turn-on time is $t_{on} = t_d + t_{fv}$.

The turn-on delay time for a given thyristor decreases as the supporting anode voltage at turn-on is increased. The delay time is also decreased by increased gate current magnitude. The gate p-region width dominates the high gate current delay time characteristics while carrier recombination is the dominant factor at low gate current levels.

The anode voltage fall time is the time interval between the 90 per cent and 10 per cent anode voltage levels. The associated anode current rise characteristics are load dependent and the recurrent *di/dt* limit must not be exceeded.

As introduced in chapter 3.3.1, a thyristor can be brought into conduction by means of an anode impressed *dv/dt*, called *static dv/dt* capability, even though no gate external current is injected. The anode voltage ramp produces a displacement current according to $i = dQ/dt$ as the central junction scl charges and its width increases. The resultant displacement current flows across the cathode and anode junctions causing minority carrier emission and, if sufficient in magnitude, turn-on occurs. Static *dv/dt* capability is an inverse function of device junction temperature and is usually measured at $\hat{T}_j$.

4.6.3ii – SCR anode at turn-off

As analysed in chapter 3.3.1, once a thyristor is turned on, it remains latched-on provided

- the holding current remains exceeded
- it is forward biased.

If the supply voltage is ac, a thyristor will turn off after the supply voltage has reversed and the anode current attempts to reverse. The thyristor is thus reverse-biased and this turn-off process is called *line commutation* or *natural commutation,* as defined in chapter 7.3.4.

If the supply voltage is dc and the load is a series *L*-*C* resonant circuit, the anode current falls to zero when the capacitor is charged. The load current falls below the holding current level and the SCR turns off. This is termed *load commutation,* which is a form of load resonant switching as defined in 7.3.3.

In thyristor applications involving dc supplies and resistive/inductive loads, a thyristor once on will remain on. Neither the supply nor the load is capable of reducing the anode current to below the holding current level, or producing a reverse bias across the thyristor. Such a thyristor can be turned off only if the anode current is interrupted or forced below the holding current level. External circuitry, called a *commutation circuit,* is employed to accomplish turn-off, by reverse-biasing the thyristor and reducing the anode current to near zero. This external turn-off approach, now obsolete, is called thyristor *forced commutation*. A topological variation of the forced commutated circuitry method is called *resonant link commutation*. The gate turn-off thyristor eliminates the need for this external commutation circuitry since the GTO can be commutated from its gate using reverse gate current.

4.7 The gate turn-off thyristor

In essence, the gate turn-off (GTO) thyristor has similar ratings and characteristics to those of the conventional converter grade SCR, except those pertaining to turn-off. Both GTO turn-on and turn-off are initiated from the gate, hence the power-handling capabilities of the GTO gate are much higher than those of SCR devices.

4.7.1 Turn-on characteristics

Because of the higher p1 gate region concentration, the GTO thyristor holding current level and gate trigger requirements are somewhat larger than those of the conventional SCR. Higher anode on-state voltages also result.

At low anode current levels, a steep trailing edge at the end of the gate on-pulse may cause the GTO to unlatch even though the anode current is above the dc holding current level. For this reason, together with the fact that the cathode comprises many interdigitated islands, a continuous, dc gate on-drive is preferred. Continuous gate current prevents any cathode islands from falling out of conduction should the anode current be reduced to near the holding current level. If cathode islands should turn off prematurely and the anode current subsequently rise, the GTO no longer has its full current handling capability and overheating of specific islands could occur, leading to device destruction.

With high voltage GTO's, turn-on is like that of a high voltage npn transistor which has low gain, limiting the initial rate of rise of anode current, until the regenerative latching action has occurred. Hence an initial, high current of up to six times the steady-state gate requirement is effective for a few microseconds.

4.7.2 Turn-off characteristics

Before commencing turn-off, a minimum on-time of tens of microseconds must be observed so that the principal current may distribute uniformly between the cathode islands. This is to ensure that all cells conduct, reaching thermal sability, such that turn-off occurs uniformly in all cells, rather than being confined to a few cells, where the current to be commutated may be higher than each cell can survive.
The anode current of a GTO in the on-state is normally turned off via a low voltage source, negative gate current, I_{RG}. The negative gate current I_{GQ}, which is just sufficient to turn-off the on-state current I_T is defined as the minimum turn-off current. Turn-off amplification (equation 3.28) is defined as

$$\beta_Q = I_{TGQ} / I_{GQ} \qquad (4.37)$$

where β_Q is related to the internal construction of the GTO thyristor.

Figure 4.18 illustrates typical gate and anode turn-off waveforms for the GTO thyristor. Application of reverse gate current causes the anode current to reduce after a delay period t_s. This delay time is decreased as the reverse gate current di_{GQ}/dt increases; that is, as I_{RGM} increases and t_s decreases. Increased anode on-state current or junction temperature increases the delay time and turn-off time.

The reverse gate current prevents cathode injection and the anode current rapidly falls to the storage current level, I_{tail}. The subsequently slow current fall time, t_{tail}, is due to charges stored in regions other than the gate and cathode that are not influenced by the reverse gate current and must decrease as a result of natural recombination, producing a decaying principal anode current. Anode n^+ shorts (or a thin transparent layer) are used to accelerate the recombination process, reducing both storage current and storage time, but at the expense of reverse blocking ability and on-state voltage. Avalanche of the cathode junction (typically -20V) is acceptable during turn-off for a specified time. Reverse gate bias should be maintained in the off-state in order to prevent any cathode injection.

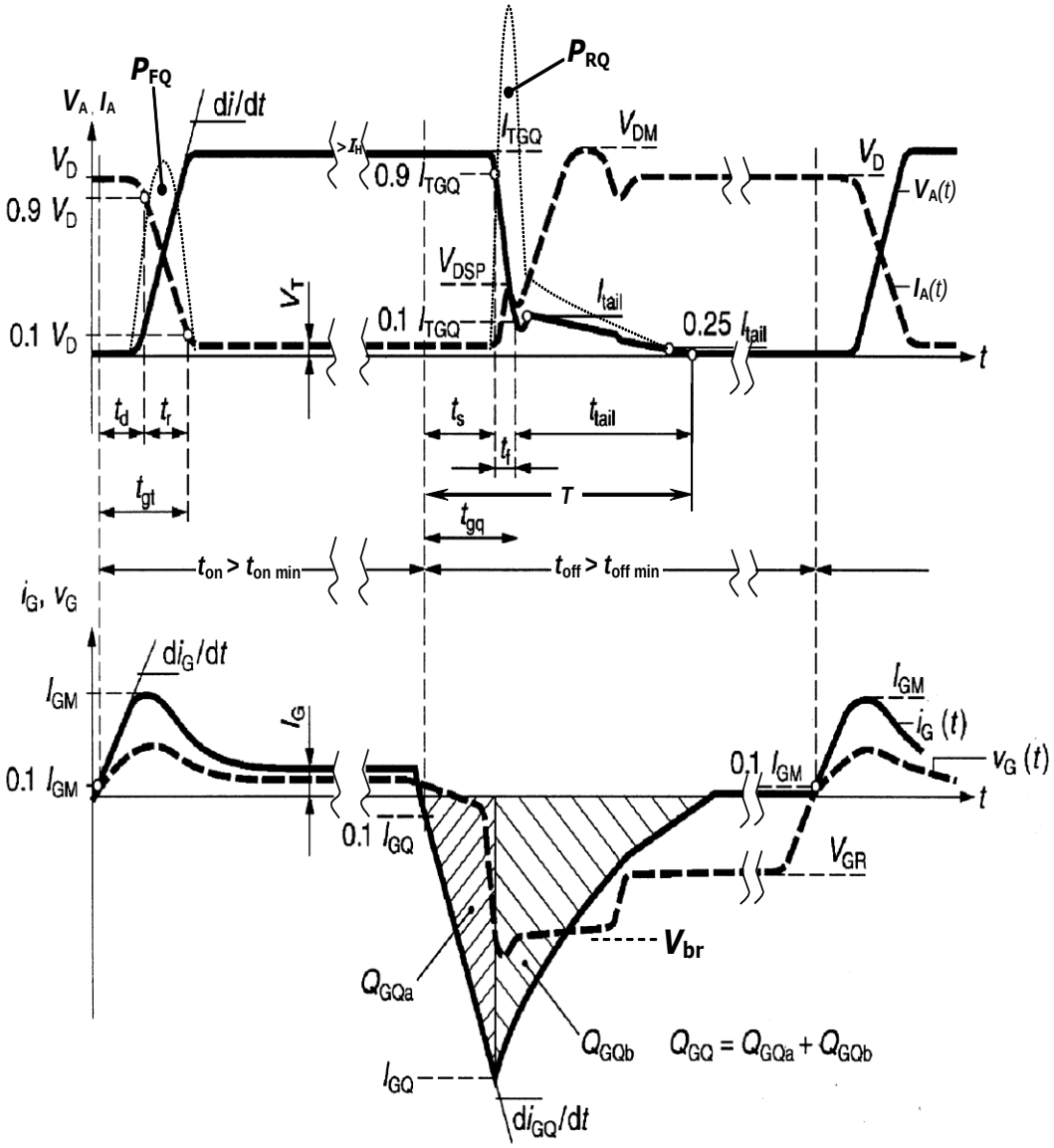

Figure 4.18. *Schematic representation of GTO thyristor turn-off waveforms.*

After turn-off some dispersed charges still exist. A minimum off-time of the order of tens of microseconds is needed for these charges to recombine naturally. This time increases with increased blocking voltage rating. If turn-on were to be initiated before this recombination were complete, the area of un-combined charge would turn-on first, resulting in a high *di/dt* in a confined area, which may cause a hot spot and possibly destruction.

During the storage and fall time, power loss P_{RQ} occurs as illustrated in figure 4.18 and is given by

$$P_{RQ} = \frac{1}{T}\int_0^T V_A(t)\ I_A(t)dt \qquad \text{(W)} \qquad (4.38)$$

where $T = t_{gq} + t_{tail}$. The cathode junction loss, due to the gate turn-off reverse current can also be incorporated, which may become significant as the turn-off gain reduces to unity.

The actual anode voltage turn-off waveform is dependent on the load circuit. Care is needed in preventing excessive loss at turn-off, which can lead to device destruction. One technique of minimising turn-off loss is to increase the rate at which the reverse gate current is applied. Unfortunately, in reducing the turn-off time, the turn-off current gain β_Q is decreased, from typically 25 to 3. The anode turn-off voltage $V_A(t)$ in figure 4.18 assumes a capacitive turn-off snubber is used. Such a capacitive switching aid circuit is not essential with the GCT, which uses unity reverse gain at turn-off, as considered in chapter 3.3.5.

4.8 Appendix: Effects on MOSFET switching of negative gate drive

The effects of negative gate voltage on MOSFET turn-on and turn-off delays, which were analysed in section 4.4.2, are given by

$$V_{gs}(t) = (V_{gg} - V_{gg-})\,[1 - e^{-t/C_{in}R_g}] + V_{gg-} \quad \text{(V)} \tag{4.39}$$

$$t_{d\,on} = R_g C_{in}\, \ell n \frac{V_{gg} - V_{gg-}}{V_{gg} - V_{TH}} \quad \text{(s)} \tag{4.40}$$

$$V_{gs}(t) = (V_{gg} - V_{gg-})\, e^{-t/R_g C_{in}} + V_{gg-} \quad \text{(V)} \tag{4.41}$$

$$t_{d\,off} = R_g C_{in}\, \ell n \frac{V_{gg} - V_{gg-}}{V_{TH} + I_L / g_{fs} - V_{gg-}} \quad \text{(s)} \tag{4.42}$$

Problems

4.1 For the mosfet, complete

i. A mosfet is a …… controlled ….. carrier device.
ii. An enhancement type of mosfet is a normally ….. device while a depletion type mosfet is a normally …. device.
iii. The mosfet gate is isolated from the principle current path by a thin layer of …… .
iv. The mosfet has a parasitic …… within its structure.
v. The gate – source voltage at which the mosfet ….. layer is formed is called the …… voltage.
vi. The length of the …. layer remains constant as the gate source voltage increases beyond the …. voltage.

[(i) voltage, majority; (ii) off, on; (iii) SiO_2; (iv). bjt/diode; (v) inversion, threshold (vi) depletion, threshold]

4.2 What is the main structural difference between a mosfet and an igbt. What are the electrical consequences?
[p+ diffusion into the mosfet drain changes the devices from a majority carrier device to a minority carrier device. Consequences are collector side minority carrier injection which gives lower on-state voltage for an igbt, but at the expense of slower switching times.]

4.3 For the mosfet and/or igbt, complete

i. A mosfet operates in the ….. mode when $V_{gs}<V_{gs\,th}$.
ii. For a mosfet in the Ohmic region V_{gs}-$V_{gs\,th}$ is greater than …… .
iii. Mosfet $R_{ds\,on}$ …… with increasing V_{gs}.
iv. In the active operational region the drain current i_d is only a function of ….. and is independent of ….. .
v. Mosfet primary breakdown is …… of drain current.
vi. Unlike the igbt and bjt, the mosfet does not undergo …….. …… .
vii. The mosfet ….. temperature coefficient of Rds facilitates easy ….. of die.
viii. For a mosfet the relationship between i_d and V_{gs}-$V_{gs\,th}$ is near …… in the active mode.
ix. Mosfet safe operating area V-I bounds is restricted by …….. .

[(i) cut-off; (ii) V_{ds}; (iii) decreases (iv) V_{gs}, V_{ds}; (v) Independent; (vi) second breakdown; (vii) positive, paralleling; (viii) linear; (ix) $R_{ds\,on}$.]

4.4 For the mosfet and/or igbt, complete

i. Mosfet and IGBT gate to source/emitter capacitance is …….. of the three terminal capacitances.
ii. Mosfet gate-drain transfer capacitance is larger in the …. region than in the …… region.
iii. During mosfet turn-on the gate – source voltages rises from zero to the ….. voltage.
iv. Mosfet voltage fall time is …… proportional to gate charging resistance.

[(i) largest; (ii) Ohmic, active; (iii) threshold; (iv) inversely.]

Reading list

See Chapter 3 reading list

Van Zeghbroeck, B., *Principles of Semiconductor Devices,* //ece-www.colorado.edu/~bart/book, 2004.

Power device manufacturers

http://www.infineon.com/eupec/toc.htm
http://www.fujielectric.co.jp/eng/fdt/scd/index.html
http://www.irf.com/indexsw.html
http://www.onsemi.com/
http://www.pwrx.com/
http://www.st.com/stonline/products/families/transistors/transistors.htm
http://www.ixys.com/
http://www.microsemi.com/
http://www.semikron.com/
http://www.fairchildsemi.com/index2.html
http://www.dynexsemi.com/
http://www.westcode.com/products.html
http://www.infineon.com/cgi-bin/ifx/portal/ep/home.do?tabId=1
http://www.abb.com/product/us/9AAC910029.aspx?country=00
http://www.mitsubishichips.com/Global/products/power/index.html
http://www.semicon.toshiba.co.jp/eng/
http://www.nxp.com/products/power_management/index.html

http://www.cree.com/
http://semisouth.com/power-semiconductors
http://www.genesicsemi.com/
http://www.rohm.com/web/global/groups/-/group/groupname/SiC%20Power%20Devices

blank