CHAPTER 24

HVDC Transmission Modelling

The analysis, design, and practical implementation of power electronics systems without computer simulation can be problematic and time consuming and therefore expensive. Consequently modelling and computer simulation play an important role in the design and analysis of complex systems. Efficient software for analysis is necessary to design and verify control algorithms in both the continuous and discrete time domains. Power electronic systems involve widely varying time constants, of over six orders, ranging from sub-microsecond semiconductor switching to 50/60Hz ac mains fluctuations. There are essentially two approaches to the modelling and simulation of a switching power converter.

One modelling method is to approximate the non-linear, discrete waveforms with fundamental frequency sinusoidal signals. This method is called an average basis technique and its main criterion is to linearize the switching circuit by creating a small-signal model and to consider the average behaviour of the switched circuit over a period. The method is used in the system implementation in this chapter. The inverters/converters and their coupling filter are modelled in a space-state formulation with the power devices within the converters represented as ideal switches. These assumptions result in some loss of detailed accuracy but the simulation time is reduced; both the time required to set up and analyze a simulation system model.
The second modelling approach treats the system on a transient time domain analysis basis, as with PSpice, EMTP, SABER, and Simulink/PLECS. The switch voltage drops and reactive components are embedded in the analysis. This method is essentially for device switching and conduction loss assessment, and to test the properties and characteristic requirements of system components.

In this chapter, the study and analysis of high voltage dc (HVDC) transmission system control algorithms are considered, rather than system efficiency and device switching parasitic effects.

24.1 Main system components

The basic structure of a voltage source converter, VSC, based HVDC system is shown in figure 24.1. The function and design of the major power components were summarised in Chapter 23, and modelling aspects follow.

24.1.1 AC circuit breaker

The ac circuit breaker, CB in figure 24.1 at the point of common coupling PCC, is used to connect and disconnect the VSC-HVDC system during normal and fault conditions. During an LCC dc fault, the ac circuit breaker disconnects the grid to prevent feeding the fault from the converter ac side. Unlike LCC HVDC, a VSC-based system has no inherent ability to isolate or clear dc link faults. The ac CB is usually modelled as low resistance in the on state and high impedance in the open state, with ideal opening and closing normally synchronised to ac zero current crossover within the block model.

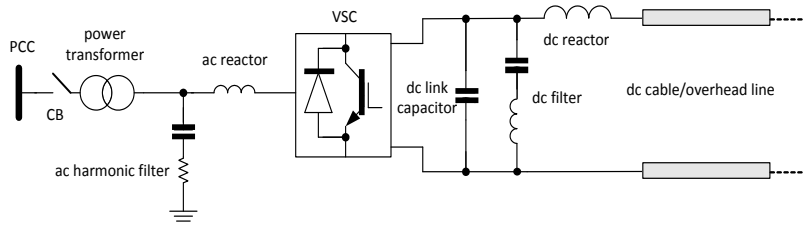


Figure 24.1. *Symmetrical mono-polar VSC-HVDC transmission system based on a two-level converter.*

24.1.2 Power converter

A three-phase voltage source converter, VSC, consists of six switches and six diodes. The main assumption in modelling is that the power switches are ideal, thus semiconductor device switching and conduction losses are neglected. Voltage source converter switch modulation has been modelled in detail in simulation software such as PSCAD and Matlab/Simulink. These models can be used for two-terminal HVDC, FACTS, and in general, for a small number of converters in a system. In a large dc grid network, which may include many VSCs, each converter has a separate controller, and has associated cable and main circuit dynamics. If the converter switching model is detail, the model becomes complex and the simulation time may become unacceptably lengthy. Start-up issues are particularly challenging as is the interaction between converter dynamics.

24.1.3 Power filter

A key system element to be modelled is the three-phase power filter as it involves most of the system control states. Its modelling is therefore important for control algorithm assessment. Figure 24.2 shows a three-phase power filter, comprised of three inductors with series loss/damping resistors and three star-connected phase shunting capacitors.

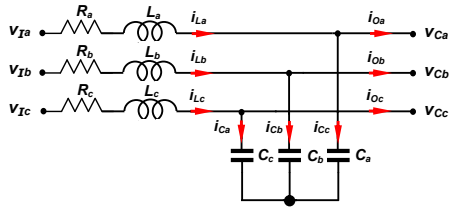


Figure 24.2. *Three-phase LC power filter model.*

Three-phase filter modelling can involve splitting it into three independent single-phase filters, with no coupling between the phases. The filter model input variables are the inverter phase voltages, v_I, and output phase currents, i_0. The model output variables, the grid side, are the phase inductor currents, i_L, and the phase capacitor voltages, v_C. To assess system robustness, the filter can be assumed unbalanced, where the components in each phase need not be equal valued. The three-phase filter model represents a sixth-order system, where the state variables are inductor currents (i_{La}, i_{Lb}, i_{Lc}) and capacitor voltages (v_{Ca}, v_{Cb}, v_{Cc}). In figure 24.2, using Kirchhoff's voltage and current laws, the relationship between the inputs, the states, and the outputs are described by (24.1) and (24.2), for phase *a*, (assuming equal capacitances *C* and equal inductances *L*):

$$v_{Ia} = Ri_{La} + L\frac{di_{La}}{dt} + v_{Ca} \tag{24.1}$$

$$i_{La} = i_{Oa} + C\frac{dv_{Ca}}{dt} \tag{24.2}$$

These differential equations for phase *a*, in state-space form, are:

$$\begin{pmatrix} i_{La} \\ v_{Ca} \end{pmatrix}' = \begin{pmatrix} -\frac{R}{L} & \frac{1}{L} \\ \frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} i_{La} \\ v_{Ca} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{pmatrix} \begin{pmatrix} v_{Ia} \\ i_{Oa} \end{pmatrix} \tag{24.3}$$

24.1.4 Power transformer

For isolation and voltage matching purposes, the VSC sub-system is connected to the grid or local network via an isolating transformer. In so doing, dc components are eliminated from the generated voltage. The transformer impedance can be used to reduce undesired harmonic contents from the output current spectrum. A *Δ/Y* transformer is used as shown in figure 24.3a, which eliminates any third harmonic flux induced component. The *Y* connection is used on the higher voltage side, thereby minimising the transformer phase voltage. A single phase equivalent circuit of the isolating transformer for the low power range is shown in figure 24.3b. The primary winding Cu resistance and leakage inductance are R_1 and L_1, respectively, while the secondary winding components referred to primary, Cu resistance and leakage inductance, are R_2 and L_2, respectively. L_m represents core magnetizing inductance and R_{e+h} represents magnetic (hysteresis) losses plus core (eddy current) losses. The shunt impedance is significantly larger than the series impedance, thus the magnetizing branch impedance can be neglected and the model is approximated as in figure 24.3c.

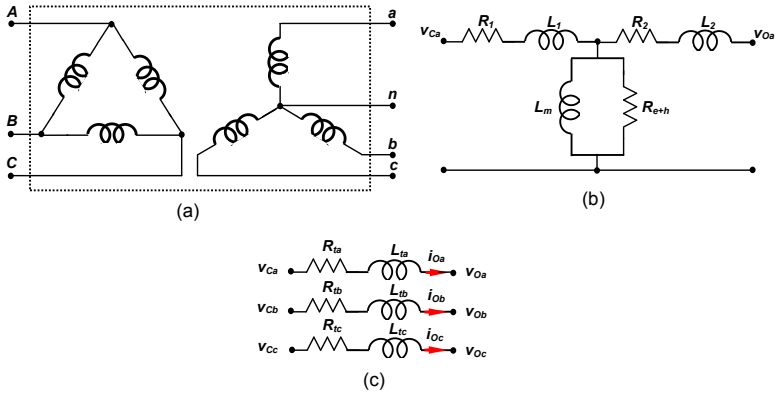


Figure 24.3. *Delta-star, Δ/Y, three-phase transformer: (a) transformer configuration; (b) single-phase equivalent circuit; and (c) approximation model.*

The transformer model equation is:

$$v_{Ca} = R_{ta} i_{Oa} + L_{ta} \frac{di_{Oa}}{dt} + v_{Oa} \tag{24.4}$$

$$i'_{Oa} = -\frac{R_{ta}}{L_{ta}} i_{Oa} + \frac{1}{L_{ta}} (v_{Ca} - v_{Oa}) \tag{24.5}$$

Transformer connection effects are included in the modelling by rearranging the equations, accounting for line and phase transformations. Figure 24.4 shows the three-phase transformer in a delta-star connection, indicating each phase current direction. This transformer connection is modelled by equations (24.6) and (24.7).

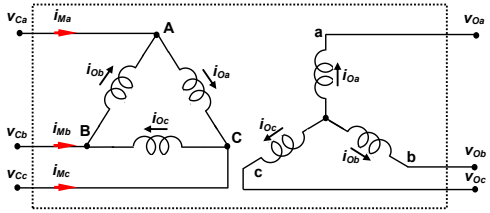


Figure 24.4. *Δ/Y three-phase transformer with phase current direction.*

$$\begin{aligned} i_{Ma} &= i_{Oa} - i_{Ob} \\ i_{Mb} &= i_{Ob} - i_{Oc} \\ i_{Mc} &= i_{Oc} - i_{Oa} \end{aligned} \tag{24.6}$$

$$\begin{aligned} v_{Ca} - v_{Cc} &= v_{Ma} \\ v_{Cb} - v_{Ca} &= v_{Mb} \\ v_{Cc} - v_{Cb} &= v_{Mc} \end{aligned} \tag{24.7}$$

24.1.5 Converter PWM modelling

A modelling solution is to develop converter average models for typical high-power converter topologies, using equivalent equations which avoid device switching, thereby allowing simulation platforms to run with acceptable simulation times. Outside the converter, the model retains the full dynamics of the system components (cables, inductors, etc.), which allows control and monitoring of system dynamics.

Assuming an ideal ac sine waveform, the model for a two-level VSC, in the *abc* frame, is:

$$\begin{aligned} V_{ac} &= ½ V_{dc} M \\ V_{ac\,m} \cos(\omega_e t + \theta_{ac}) &= ½ V_{dc} M_m \cos(\omega_m t + \theta_m) \end{aligned} \tag{24.8}$$

where the input control signal is $M = M_m \cos(\omega_m t + \theta_m)$, thus the three input control signals are M_m, ω_m and θ_m. From equation (24.8), $M_m = 4V_{dc} / \sqrt{2}\,\pi$. Similar equations result for phases *b* and *c*. In the *dq* frame, rotating at the fundamental frequency, the model reduces to:

$$V_a = ½ V_{dc} M_a \qquad V_b = ½ V_{dc} M_b \qquad V_c = ½ V_{dc} M_c \tag{24.9}$$

From system power balance

$$\begin{aligned} P_{dc} &= P_{ac} \\ V_{dc} I_{dc} &= I_a V_a + I_b V_b + I_c V_c \\ I_{dc} &= ½ (I_a M_a + I_b M_b + I_c M_c) \end{aligned} \tag{24.10}$$

where M_a, M_b and M_c are the model input control signals for the respective phases, while V_a, V_b, V_c and I_{DC} are the model output voltages and current. The converter is a controllable voltage source on the ac side, and a controllable current source on the dc side. Figure 24.5 shows the Matlab/Simulink implementation of the VSC model. Averaged models adequately represent the dominant system dynamics and are sufficiently accurate for designing the main HVDC control loops, being generally suitable in the frequency range below 60-100Hz.

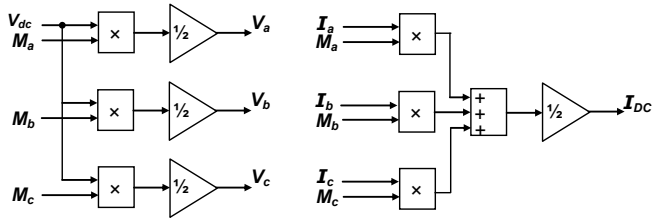


Figure 24.5. *Implementation of the VSC averaged model.*

24.2 VSC HVDC ac power flow control - HVDC PQ operating diagrams

The VSC exchanges power with the ac grid through an interconnecting reactor, by controlling the converter ac voltage, as shown in figure 24.6. The ac voltages V_g and V_c, in the rotating *dq* frame, are:

$$\bar{V}_g = V_{gm} \angle \alpha_g = V_{gd} + jV_{gq} \tag{24.11}$$

$$\bar{V}_c = V_{cm} \angle \alpha_c = V_{cd} + jV_{cq} \tag{24.12}$$

where $\bar{V}_g$, $\bar{V}_c$ are phasors, V_{gm}, V_{cm} are the magnitudes and α_g, α_c are phase angles of the respective phasor voltages. The subscripts *d* and *q* denote the corresponding phasor *dq* components. A phase locked loop, PLL, is used to synchronise the reference frame with the point of common coupling, PCC, voltage. Without loss of generality, V_g is locked on *d*-axis, $\alpha_g = 0$, then:

$$\bar{V}_g = V_{gd} = V_{gm}, \quad V_{gq} = 0 \tag{24.13}$$

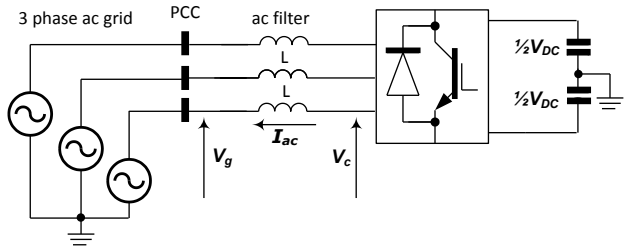


Figure 24.6. *Three-phase ac-dc VSC connected to the ac grid.*

In this topology, the converter voltage V_c is controlled by sinusoidal PWM, and the converter line to neutral rms voltage is:

$$V_{cd} = M_{cd}\frac{V_{dc}}{2\sqrt{2}} \qquad V_{cq} = M_{cq}\frac{V_{dc}}{2\sqrt{2}} \qquad M_c = \sqrt{M_{cd}^2 + M_{cq}^2} \tag{24.14}$$

where M_{cd}, M_{cq} are the *dq* components of the sinusoidal PWM control signal and V_{dc} is the dc link voltage. The circuit equation across the interface filter and transformer, with total inductance *L*, is:

$$j\omega L\bar{I}_{ac} = jX_L\bar{I}_{ac} = \bar{V}_c - \bar{V}_g \tag{24.15}$$

where $\omega=2\pi f$ in which the grid frequency is $f = 50/60Hz$. Equation (24.15) in terms of individual current components, is:

$$\bar{I}_{ac} = I_{acd} + jI_{acq} = \frac{V_{cd} + jV_{cq} - V_{gm}}{jX_L} \tag{24.16}$$

From equation (24.16), current I_{ac} has a similar 'sensitivity' to the converter voltages V_c and V_g.

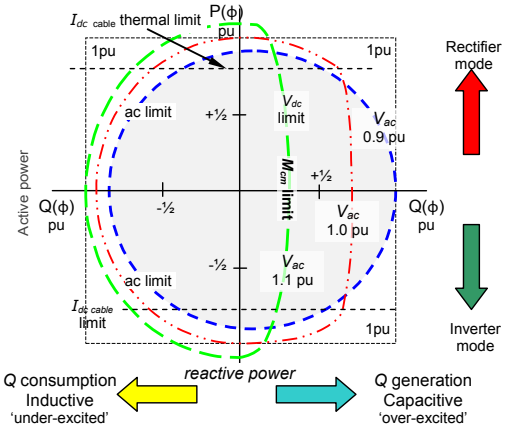


Figure 24.7. *Active and reactive power capability control locus.*

The PCC complex power of the VSC into the interfacing inductor *L* shown in figure 24.6, is:

$$S_g = 3\bar{V}_g\,\bar{I}_{ac}^{*} = 3\bar{V}_g\left[\frac{\bar{V}_c - \bar{V}_g}{j\omega L}\right]^{*} = 3\bar{V}_g\left[\frac{\bar{V}_c - \bar{V}_g}{jX_L}\right]^{*} \tag{24.17}$$

Substituting equations (24.11) and (24.12) into (24.17) yields

$$S_g = 3V_{gm}\left[\frac{V_{cq}}{\omega L} - j\frac{V_{cd} - V_{gm}}{\omega L}\right]^{*} = 3\frac{V_{gm}}{X_L}\left[V_{cq} - j\left(V_{cd} - V_{gm}\right)\right]^{*} \tag{24.18}$$

$$P_g = 3V_{gm}\frac{V_{cq}}{X_L} \qquad Q_g = 3V_{gm}\frac{V_{cd} - V_{gm}}{X_L}$$

Typical *P*-*Q* curves are shown in figure 24.7, along with the associated modulation indices.

24.3 VSC: vector control, coordinate frame transformation, inner decoupled current control

At the control system level, VSCs have similar input-output structures and can be viewed as two-input, two-output, non-linear, dynamic amplifiers. The converter control inputs are employed to develop feedback regulators to achieve various control functions, depending on the converter application.

A VSC controller should fulfil the following control goals:

- Regulate the controlled variables. Some of the variables regulated to a reference are:
  - dc voltage, to ensure minimum losses and to prevent insulation damage;
  - power transfer, according to scheduling demands;
  - reactive power exchange; and
  - ac voltage level, which is important with weak (high impedance) ac grids.
- Protect a converter from damage caused by currents or voltages exceeding rated values.
- Ensure system stability and good response speed - implying bounded responses and good transient performance of system variables under all foreseen operating conditions and disturbances.
- Local ac grid support. Typically with weak, low-inertia ac grids, the VSC frequency stabilises using frequency droop feedback. With high-impedance systems, voltage stabilisation may be required.

These control functions are normally achieved with two-level cascaded converter control where inner loop control ensures protection and stability while outer loop control fulfils performance goals. Inner loops normally use fast decoupled current control. The outer loop controller achieves various regulation and stabilisation functions by providing references to the inner current control loops.
Such a control structure has evolved from the controllers used with VSCs in variable speed drives. The main difference is the HVDC VSC large size which impacts on the ac grid. Additionally, the HVDC VSC may be connected to long dc cables, whence dc system dynamics play an important role.
Converter gating circuit level control depends on the converter type. Without loss of generality, it is assumed that sinusoidal pulse width modulation (SPWM) is used with two-level converters, as considered in Chapter 17.1.3v. Gating synchronisation is achieved with a PLL.
VSC control is based on appreciation of the converter inner dynamics, consequently detailed converter modelling is an initial step. VSC modelling uses a per-phase dynamic model and converts this into the rotating coordinate frame, assuming a symmetrical, balanced three-phase system.

24.3.1 Converter and ac grid model in static frame

Figure 24.8 shows the basic schematic of a VSC connected to a local 50/60Hz ac grid.

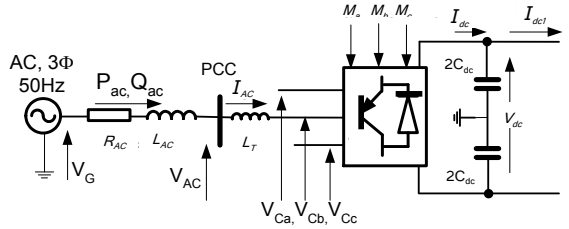


Figure 24.8. *A VSC connected to a local ac grid.*

V_G equivalent remote source voltage (fixed magnitude, grid)
V_{AC} local point of (common) connection voltage, PCC (voltage for PLL synchronisation)
V_C converter ac voltage
V_{dc} converter dc voltage
I_{AC} ac-side line current
I_{DC} converter dc current
I_{DC1} current from the dc grid

The converter control signals (in a static frame) are M_a, M_b, and M_c. The parameters R_{AC} and L_{AC} represent the equivalent grid impedance, whilst L_T is the transformer (and/or inductor) reactance. The dynamic equations for the three phases (*a*, *b* and *c*) in a static coordinate frame, with $L_\Sigma = L_{AC} + L_T$, are:

$$\begin{aligned} v_{Ga} &= v_{Ca} + R_{AC} i_{ACa} + L_\Sigma \frac{di_{ACa}}{dt} \\ v_{Gb} &= v_{Cb} + R_{AC} i_{ACb} + L_\Sigma \frac{di_{ACb}}{dt} \\ v_{Gc} &= v_{Cc} + R_{AC} i_{ACc} + L_\Sigma \frac{di_{ACc}}{dt} \end{aligned} \tag{24.19}$$

The complex ac power equation, at the point of coupling, is:

$$S_{AC} = v_{ACa} i_{ACa} + v_{ACb} i_{ACb} + v_{ACc} i_{ACc} \tag{24.20}$$

Assuming a two-level SPWM controlled converter, the converter model is:

$$\begin{aligned} v_{Ca} &= \tfrac{1}{2} M_a V_{dc} \\ v_{Cb} &= \tfrac{1}{2} M_b V_{dc} \\ v_{Cc} &= \tfrac{1}{2} M_c V_{dc} \end{aligned} \tag{24.21}$$

The high voltage dc circuit equation is:

$$i_{DC} = C_{dc} \frac{dv_{dc}}{dt} + i_{DC1} \tag{24.22}$$

24.3.2 Converter and ac grid model in a rotating coordinate frame

Park's transformation is used to convert the applicable equations into a synchronously rotating *dq* reference frame. With a symmetrical, balanced system, the equations in (24.19) transform to:

$$\begin{aligned} v_{gd} &= v_{Cd} + R_{AC} i_{ACd} - \omega_e L_\Sigma i_{ACq} + L_\Sigma \frac{di_{ACd}}{dt} \\ v_{gq} &= v_{Cq} + R_{AC} i_{ACq} + \omega_e L_\Sigma i_{ACd} + L_\Sigma \frac{di_{ACq}}{dt} \end{aligned} \tag{24.23}$$

where ω_e is electrical system frequency, rad/s, and *d*, *q* subscripts represent the coordinate frame axes.

The ac power equation (24.20) in the rotating frame becomes:

$$\begin{aligned} S_{AC} &= P_{AC} + jQ_{AC} = \tfrac{3}{2}\left(v_{ACd} + j\, v_{ACq}\right)\left(i_{ACd} - j\, i_{ACq}\right) \\ P_{AC} &= \tfrac{3}{2}\left(v_{ACd} i_{ACd} + v_{ACq} i_{ACq}\right) \qquad Q_{AC} = \tfrac{3}{2}\left(-v_{ACd} i_{ACq} + v_{ACq} i_{ACd}\right) \end{aligned} \tag{24.24}$$

The converter model, the equations in (24.21), transform as:

$$\begin{aligned} v_{Cd} &= \tfrac{1}{2} M_{Cd} V_{dc} \\ v_{Cq} &= \tfrac{1}{2} M_{Cq} V_{dc} \end{aligned} \tag{24.25}$$

The converter active power on the ac side, using (24.24), is:

$$P_C = \tfrac{3}{2}\left(v_{Cd} i_{ACd} + v_{Cq} i_{ACq}\right) \tag{24.26}$$

The converter dc side power is

$$P_{DC} = V_{dc} i_{DC} \tag{24.27}$$

Equating (24.26) and (24.27), and using equation (24.25), the expanded power balance equation is:

$$\tfrac{3}{2}\left(\tfrac{1}{2} M_{Cd} i_{ACd} V_{dc} + \tfrac{1}{2} M_{Cq} i_{ACq} V_{dc}\right) = V_{dc} i_{DC} \tag{24.28}$$

From (20.11), the converter dc current can be expressed as:

$$i_{DC} = \tfrac{3}{4}\left(M_{Cd} i_{ACd} + M_{Cq} i_{ACq}\right) \tag{24.29}$$

4.3.3 Inner current controller design

Assume that the coordinate frame is aligned (using a PLL) with the ac terminal voltage, that is, the voltage vector V_{AC} is located on the *d* axis. Then $v_{ACq} = 0$ and the equations in (24.24) become:

$$P_{AC} = \tfrac{3}{2} v_{ACd} i_{ACd} \qquad Q_{AC} = -\tfrac{3}{2} v_{ACd} i_{ACq} \tag{24.30}$$

By maintaining the terminal voltage near the rated value, the terminal voltage influence can be neglected, that is, $v_{ACd} = constant$. From equation (24.30), the active and reactive powers by controlling i_{ACd} and i_{ACq}, respectively. The simplicity of the equations in (24.30) is a reason for using *dq* current control in the fast inner controller. The second reason is that direct current control can prevent converter overheating, particularly during fault conditions. Substituting (24.25) into the equations in (24.23):

$$\begin{aligned} v_{gd} &= \tfrac{1}{2} M_{Cd} V_{dc} + R_{AC}\, i_{ACd} - \omega_e L_\Sigma i_{ACq} + L_\Sigma \frac{di_{ACd}}{dt} \\ v_{gq} &= \tfrac{1}{2} M_{Cq} V_{dc} + R_{AC}\, i_{ACq} + \omega_e L_\Sigma i_{ACd} + L_\Sigma \frac{di_{ACq}}{dt} \end{aligned} \tag{24.31}$$

where the control signals M_{Cd} and M_{Cq} can manipulate converter currents I_{ACd} and I_{ACq}, respectively, but cross coupling terms exist. Therefore decoupled control loops are introduced:

$$M_{Cd} = 2\frac{M_{Cd1} + L_\Sigma \omega_e\, i_{ACq}}{V_{dc}} \qquad M_{Cq} = 2\frac{M_{Cq1} - L_\Sigma \omega_e\, i_{ACd}}{V_{dc}} \tag{24.32}$$

M_{Cd1} and M_{Cq1} are control signals from the main feedback current loops. The current signals i_{ACd} and i_{ACq} in the decoupling loops in the equations in (24.32) are wide bandwidth measurements to account for their fast dynamics, having widely varying magnitudes during normal operation. V_{dc} is not normally used in the feedback loop since the dc voltage is usually tightly controlled: $V_{dc} = constant$. Substituting the equations in (24.32) into the equations in (24.31) yields:

$$v_{gd} = M_{Cd1} + R_{AC}\, i_{ACd} + L_\Sigma \frac{di_{ACd}}{dt} \qquad v_{gq} = M_{Cq1} + R_{AC}\, i_{ACq} + L_\Sigma \frac{di_{ACq}}{dt} \tag{24.33}$$

In these two equations, there are two control signals, M_{Cd1} and M_{Cq1}, controlling two independent variables i_{ACd} and i_{ACq} under external disturbances v_{Gd} and v_{Gq}. The controller design reduces to two independent first order systems.

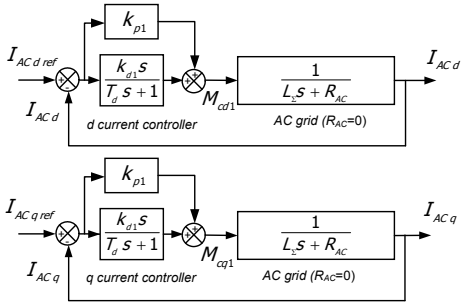


Figure 24.9. *Design of the two inner current feedback loops.*

In power systems, the line resistance R_{AC} is typically small and $X_{AC}/R_{AC} > 10$. As an initial approximation assume $R_{AC} = 0$; then the system in equation (24.33) has a predominantly integral behaviour. An integral system is normally controlled with a PD (proportional differential) type controller for good performance and zero tracking error. The dynamic equations of the PD controller, in the Laplace domain, are:

$$M_{cd1} = (k_{p1} + \frac{s\,k_{d1}}{T_d s + 1})(i_{ACd\,ref} - i_{AC\,d}) \qquad M_{cq1} = (k_{p1} + \frac{s\,k_{d1}}{T_d s + 1})(i_{ACq\,ref} - i_{AC\,q}) \tag{24.34}$$

where k_{p1} and k_{d1} are the controller proportional and differential gains, respectively and T_d is a filter constant associated with the small differential term. Figure 24.9 shows the inner control loops in the schematic of the decoupled system.

Substituting equations (24.34) into (24.33), and neglecting disturbances, the closed loop system is:

$$i_{ACd} = \frac{\left(k_{p1}T_d + k_{d1}\right)s + k_{p1}}{L_\Sigma T_d s^2 + \left(L_\Sigma + k_{p1}T_d + k_{d1}\right)s + k_{p1}} i_{ACd\,ref} \qquad i_{ACq} = \frac{\left(k_{p1}T_d + k_{d1}\right)s + k_{p1}}{L_\Sigma T_d s^2 + \left(L_\Sigma + k_{p1}T_d + k_{d1}\right)s + k_{p1}} i_{ACq\,ref} \tag{24.35}$$

Since the differential time constant is small compared with the dominant dynamics, assuming $T_d = 0$, the equations in (24.35) become:

$$i_{ACd} = \frac{k_{d1}s + k_{p1}}{(L_\Sigma + k_{d1})s + k_{p1}} i_{ACd\,ref} \qquad i_{ACq} = \frac{k_{d1}s + k_{p1}}{(L_\Sigma + k_{d1})s + k_{p1}} i_{ACq\,ref} \tag{24.36}$$

The controller gains in this system can be determined as follows. The initial value of the step response is given by k_{d1}, and the time constant is $T_I = (L_\Sigma + k_{d1}) / k_{p1}$. Therefore for a desired speed of response k_{p1} and k_{d1} can be determined. k_{p1} increases the transient response speed whereas k_{d1} slows response. However k_{d1} increases the initial value of the response. The response speed is typically limited by the dynamics of the feedback filters for current measurements in the decoupling loops in equations (24.32). With a finite system resistance R_{AC}, the controller gives a steady-state error of $R_{AC}/(R_{AC} + k_{p1})$. A small integral term k_{I1} is added in the inner control loop to eliminate this error. Non-zero R_{AC} also increases the response speed and the time constant becomes $T_{I1} = (L_\Sigma + k_{d1}) / (k_{p1} + R_{AC})$.

Since the inner control is based on current signal estimates, the impact of current measurement noise is reduced, but control is less robust to parameter variations.

24.3.4 Outer controller design

The inner control loops can be considered a fast, first order system, based on the dominant dynamics in (24.36). The outer control loops manipulate current references i_{ACdref} and i_{ACqref} to achieve higher control goals. From (24.30), the *d*-current component affects the active power while the *q*-current component affects the reactive power. The *d* current is therefore used for controlling either power transfer or the dc link voltage. The *q* current is typically manipulated to regulate the reactive power exchange or the ac voltage level.

The outer controllers are typically proportional integral (PI) types so as to ensure satisfactory response time and to eliminate tracking error.

24.3.5 AC voltage control

VSCs using ac voltage control may be attractive with weak ac systems, that is, systems with high impedance. Figure 24.10 shows an outer ac voltage control scheme assuming that only the dominant dynamics from the inner *q*-current control from figure 24.9 are present.

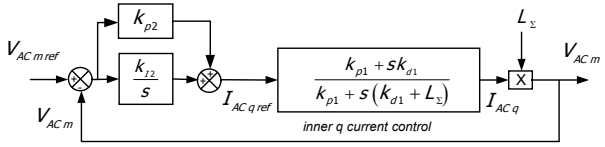


Figure 24.10. *Design of the outer ac voltage controller.*

The transfer function in figure 24.10, is:

$$V_{ACm} = \frac{\left[k_{I2}k_{p1} + s(k_{p2}k_{p1} + k_{d1}k_{I2}) + s^2 k_{p2}k_{d1}\right]L_\Sigma}{k_{p1}k_{I2}L_\Sigma + s\left[k_{p1} + (k_{p2}k_{p1} + k_{d1}k_{I2})L_\Sigma\right] + s^2\left[k_{p2}k_{d1}L_\Sigma + k_{d1} + L_\Sigma\right]} V_{AC\,m\,ref} \tag{24.37}$$

This system is a conventional second order filter. Therefore for a desired damping ratio ζ_2 and frequency ω_2 of the ac voltage control system, the two controller parameters (gains k_{p2} and k_{I2}) can be determined:

$$\omega_2^2 = \frac{k_{p1}k_{I2}L_\Sigma}{k_{p2}k_{d1}L_\Sigma + k_{d1} + L_\Sigma} \qquad 2\zeta_2\omega_2 = \frac{k_{p1} + (k_{p2}k_{p1} + k_{d1}k_{I2})L_\Sigma}{k_{p2}k_{d1}L_\Sigma + k_{d1} + L_\Sigma} \tag{24.38}$$

24.3.6 Power control

Figure 24.11 shows an outer power control system, assuming that only the dominant dynamics from the inner *d*-current control from figure 24.10 are present.

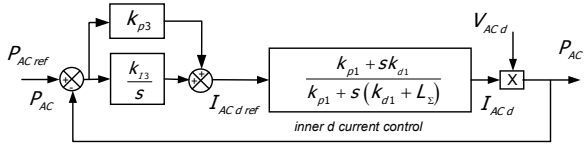


Figure 24.11. *Design of the outer power controller.*

The transfer function for figure 24.11 is:

$$P_{AC} = \frac{\left[k_{I3}k_{p1} + s(k_{p3}k_{p1} + k_{d1}k_{I3}) + s^2 k_{p3}k_{d1}\right]V_{AC\,d}}{k_{p1}k_{I3}V_{ACd} + s\left[k_{p1} + (k_{p3}k_{p1} + k_{d1}k_{I3})V_{ACd}\right] + s^2\left[k_{p3}k_{d1}V_{AC\,d} + k_{d1} + L_\Sigma\right]} P_{AC\,ref} \tag{24.39}$$

Therefore for a desired damping ratio ζ_3 and frequency ω_3, the gains k_{p3} and k_{I3} can be determined:

$$\omega_3^2 = \frac{k_{p1}k_{I3}\,V_{AC\,d}}{k_{p3}k_{d1}V_{ACd} + k_{d1} + L_\Sigma} \qquad 2\zeta_3\omega_3 = \frac{k_{p1} + (k_{p3}k_{I1} + k_{d1}k_{I3})V_{ACd}}{k_{p3}k_{d1}V_{ACd} + k_{d1} + L_\Sigma} \tag{24.40}$$

24.3.7 DC voltage control

The dc voltage equation for the scheme in figure 24.8 is:

$$C\frac{dV_{dc}}{dt} = I_{DC} - I_{DC1} \tag{24.41}$$

Since the power equations are simpler than the current equations, equation (24.41) is converted to a power equation by multiplying with V_{dc}:

$$\tfrac{1}{2}C\frac{dV_{dc}^2}{dt} = P_{DC} - P_{DC1} \tag{24.42}$$

Considering the simplicity of equation (24.42), the dc voltage controller is frequently designed to control the square of the dc voltage, rather than the dc voltage. A dc voltage controller is shown in figure 24.12.

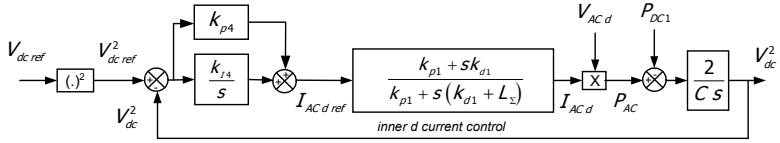


Figure 24.12. *Design of the outer dc voltage controller.*

The transfer function for the system in figure 24.12 is:

$$V_{dc}^2 = \frac{\left[k_{I4}k_{p1} + s(k_{p4}k_{p1} + k_{d1}k_{I4}) + s^2 k_{p4}k_{d1}\right]2V_{AC\,d}}{2k_{p1}k_{I4}V_{ACd} + 2s(k_{p4}k_{p1} + k_{d1}k_{I4})V_{ACd} + s^2\left(2k_{p4}k_{d1}V_{ACd} + k_{p1}\right) + s^3\left(k_{d1} + L_\Sigma\right)} V_{DC\,ref}^2 \tag{24.43}$$

This system has dominant integral dynamics which can be explained by considering the magnitude of various terms in the denominator in equation (24.43). Consequently, the system can be controlled with a PD-type controller. However because of the practical importance of accurate dc voltage regulation, integral control gain is necessary. Therefore a PI controller with gains k_{I4} and k_{p4} is used, which is typically tuned using a root locus technique. Firstly, the controller zero $z_c = k_{I4}/k_{p4}$ is determined from the controller transfer function:

$$I_{ACd\,ref} = \frac{k_{p4}s + k_{I4}}{s}(V_{dc\,ref}^2 - V_{dc}^2) = k_{p4}\frac{s + z_c}{s}(V_{dc\,ref}^2 - V_{dc}^2) \tag{24.44}$$

The zero is placed close to the dominant system pole, or close to the origin for integral systems. Next, the proportional gain is varied and the location of the poles is observed on the root locus.

24.3.8 AC grid support

The power reference in figure 24.11 is usually maintained at a scheduled constant level for a particular station. Alternatively, the power reference can be made dependent on frequency deviations in the ac grid. There are two reasons for this additional control function:

- Large VSCs in an inverting mode should be treated like any large conventional power plant. Normally large generators use frequency droop feedback as an additional signal for power regulation. In a rectifying mode, the converter can be treated as a normal ac system, non-linear load.
- For a weak, low inertia ac system, it is beneficial to modulate the VSC power exchange in response to ac system frequency deviation. This control function applies to rectification and inversion converter modes. Such control is used with conventional and VSC, HVDC systems. With VSC HVDC, frequency support can be extended to regulate the frequency on dead ac networks.

The droop gain for ac grid support is:

$$k_{AC\ droop} = \frac{2P_{DC\max}}{f_{AC\max} - f_{AC\min}} \tag{24.45}$$

where f_{ACmax} and f_{ACmin} are the allowable limits for the ac system frequency deviation and P_{DCmax} is the maximum converter power allowed for system support. If dynamic support and ac grid stabilization are needed, a dynamic feedback loop replaces the static gain $k_{AC\ droop}$, where the feedback loop has a frequency-dependent transfer function to enhance stability (phase or gain margin) with a particular frequency bandwidth.
With conventional point-to-point HVDC, the stronger ac system can dynamically support the other system. Such stabilization is achieved through HVDC control, but power is essentially drawn from the remote (stronger) ac system.

24.3.9 The complete VSC controller

The complete VSC controller is shown in figure 24.13. The schematic includes the inner current control loops, the outer loops with droop feedback, phase locked loop synchronization, and also the switch gating for SPWM at a switching frequency f_s. The outer control loops each have a switch for selecting the top-level control choice. The controller outputs are the gating signals for three-phase converter six IGBT switches (S_1 to S_6).

Stabilization of a dc grid through $k_{dc\ droop}$ is included, for both point-to-point and multi-terminal HVDC systems.

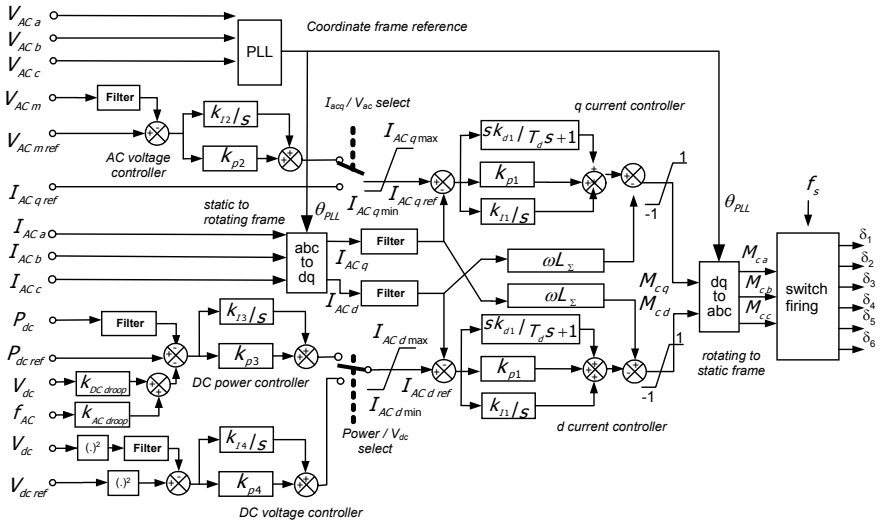


Figure 24.13. *VSC controller with inner and outer control loops.*

24.4 VSC HVDC SIMULINK controller steady-state simulation

A 275kV, 200MVA, HVDC system interconnects between two ac systems as shown in figure 24.14, where the two ac grids, and interfacing transformer parameters are shown in figure 24.14. Sinusoidal pulse width modulation (SPWM) uses a 2.1kHz triangular carrier. The dc cable is 1000mm^2 copper with a specific resistance of $R = 2.5\times10^{-2}$ Ω/km, where the total distance is 100km.
Converter station #1 controls the active power between the two ac grids, while converter station #2 regulates the dc link voltage. Also controller #2 regulates the ac voltage at PCC #2 to support the ac grid, by injecting reactive power into the ac grid.
To demonstrate four quadrant operation and voltage support capability of the VSC-HVDC system, converter station #1, as in figure 24.15, is commanded to increase its output power export from grid G_1 to G_2 from 0 to 0.9pu (180 MW) at 1.5pu/s. At time t = 1s it is commanded to reverse the active power flow in order to import 180 MW from grid G_2, at -1pu/s.

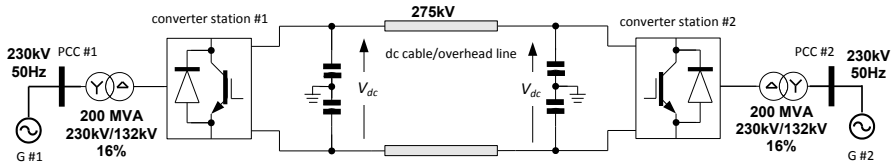


Figure 24.14. *VSC-HVDC transmission system based on two-level converters.*

Figure 24.15a presents station #1 direct and quadrature axis currents. Station #1 active power along with the reference are shown in figure 24.15b. The controller performance is acceptable and the measured powers track the required references. The magnitude and angle of the fundamental converter voltage are shown in figure 24.15c in both rectifying and inverting modes. The magnitude is constant due to zero injected reactive power. The converter control signals M_d, M_q are shown in figure 24.16. The three-phase voltages and currents are shown in figure 24.17 parts a and b, respectively. The dc link voltage is shown in figure 24.17c. Figure 24.18 parts a and b show a focused period of the three phase ac voltages and currents respectively.

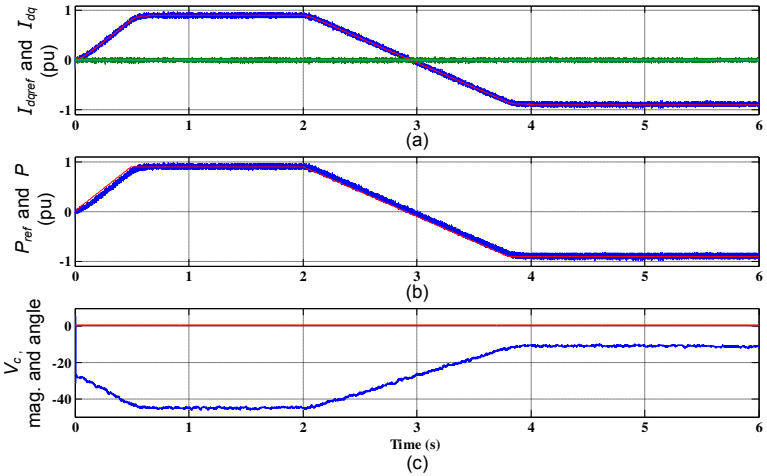


Figure 24.15. *Station #1 simulation: (a) output d-q currents and the reference, (b) active power converter exchange with PCC_1, and (c) magnitude and angle of converter #1 voltage.*

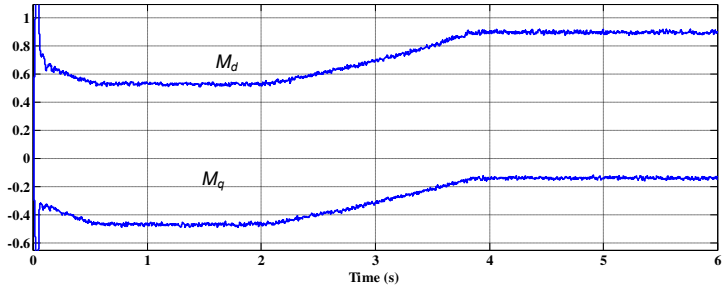


Figure 24.16. *Converter #1 control signals M_d and M_q.*

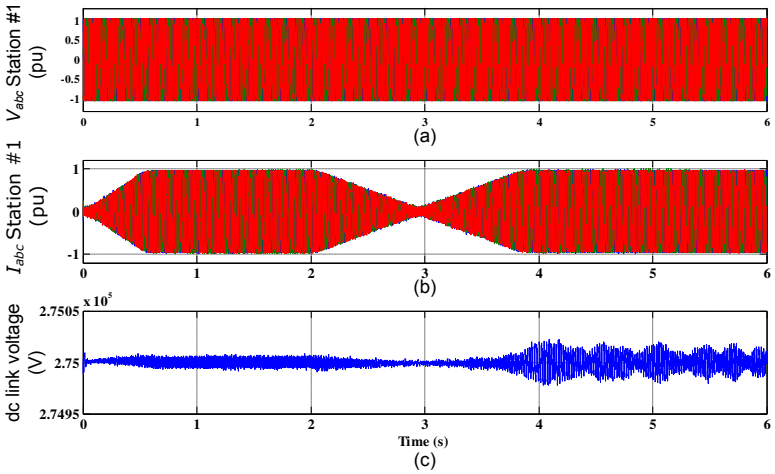


Figure 24.17. *Station #1 simulation:*
(a) three-phase grid ac voltages, (b) three-phase ac currents, and (c) dc link voltage.

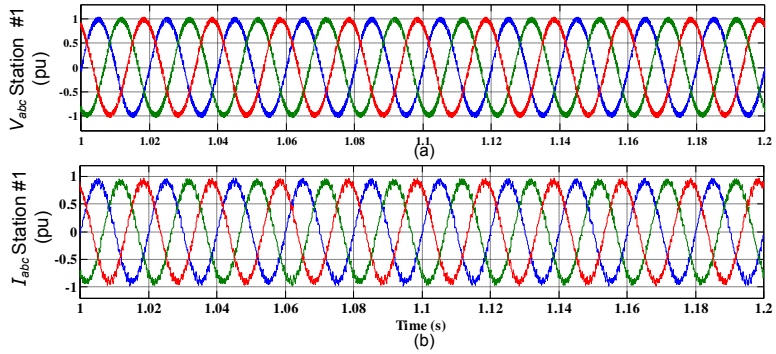


Figure 24.18. *Station #1 simulation three-phase ac: (a) voltages and (b) currents.*

The three-phase voltages and currents of station #2 are shown in figure 24.19 parts a and b, respectively. Figure 24.19c shows station #2 simulated active and reactive powers. The converter is able to adjust its reactive power exchange with PCC #2 in order to support the ac voltage during the entire operating period.
Figure 24.20a shows station #2 direct and quadrature axis currents with its references. The dc link voltage along with the reference are shown in figure 24.20b. The magnitude and angle of the fundamental converter #2 voltage are shown in figure 24.20c. Figure 24.21 parts a and b show a focused period of the three-phase ac voltages and currents respectively.

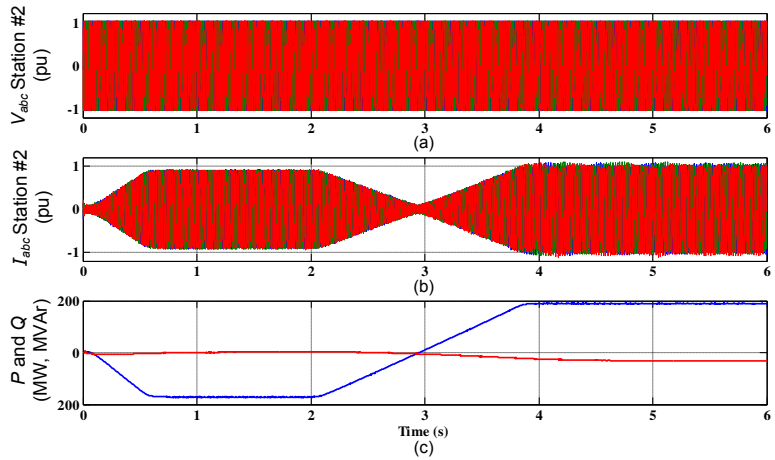


Figure 24.19. *Station #2 simulation:*
(a) three-phase grid ac voltages, (b) three-phase ac currents, and (c) active/reactive powers.

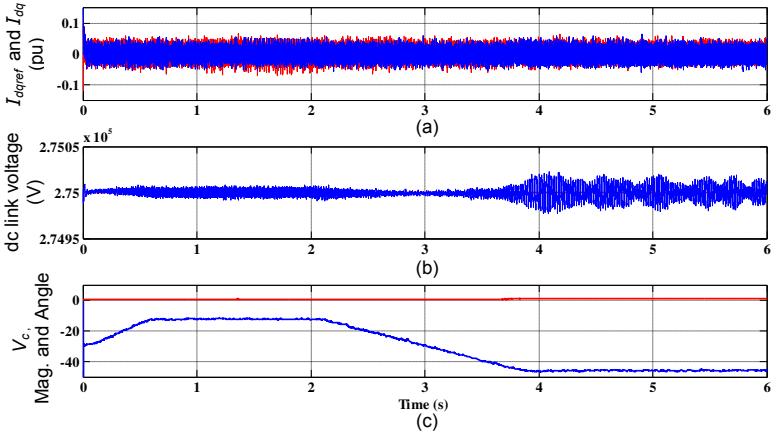


Figure 24.20. *Station #2 simulation: (a) output current d-q and its reference,*
(b) dc link voltage with its reference, and (c) magnitude and angle of the converter voltage.

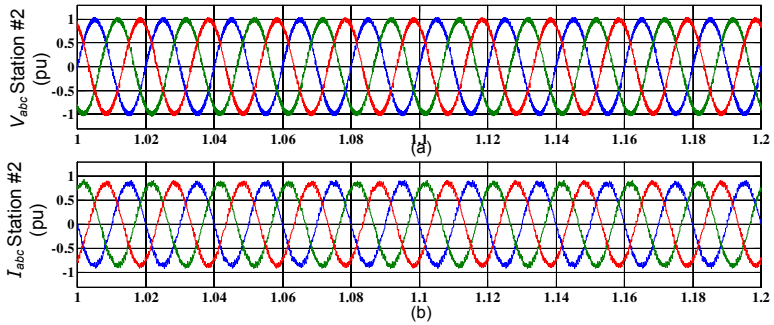


Figure 24.21. *Station #2 simulation of three-phase ac: (a) voltages and (b) currents.*

24.5 VSC HVDC SIMULINK simulation of fault conditions

In demonstrating HVDC system response to ac and dc faults, the system shown in figure 24.22 is assumed to be operating at full power prior to a fault.

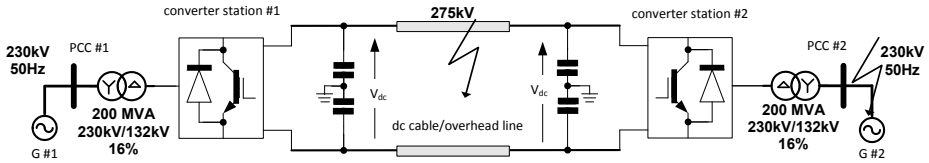


Figure 24.22. *Faulted VSC-HVDC transmission system based on two-level converters.*

24.5.1 AC faults on V_g

Converter current under an extreme fault with $V_g = 0$ can be obtained from equation (24.16) by setting $V_{gm} = 0$. In general, a converter can control this fault current by reducing the voltage V_c via the current control loops. However, the control loop has small delays, and in the instant after the fault only the inductor limits the fault current. The grid fault current magnitude I_{acm} is:

$$I_{ac\,fm} = \frac{V_{c\,m}}{\omega L} = \frac{V_{c\,m}}{X_L} \tag{24.46}$$

From this equation, large inductances limit the fault current magnitude. However large inductance results in high inductor losses and large voltage swings on V_c. The fault current magnitude should be below 2pu because applicable IGBTs have a maximum rated turn-off capability of twice the rated average current. The magnitude of ac voltage V_{cm} ($V_{cm} \approx V_{cd}$) must be close to V_{gm} in order to readily enable bidirectional reactive power. Therefore, from (24.46), the fault current can reach extreme values.

Figure 24.23 shows the output current magnitude during a three-phase fault at $t = 1$s with three different interfacing inductances.

Figure 24.24 shows the simulation of the HVDC test system when subjected to a 160ms (8 cycles for 50Hz) three-phase ac fault to ground at the inverter PCC #2 bus shown in figure 24.22. The three-phase ac voltages and currents are shown in figure 24.24. Figure 24.25a shows the active and reactive powers that converter #2 injects into PCC #2. The system is able to recover once the fault is cleared, and converter #2 adjusts its reactive power exchange with grid G #2 in order support ac voltage at PCC #2. The active and reactive power transients at PCC #2 are related to the reaction of the ac voltage controller that regulates the ac voltage at PCC #2. The dc link voltage increases because of the trapped energy in the dc side, since energy cannot be transferred as the voltage at PCC #2 collapses, as shown in figure 24.25b.

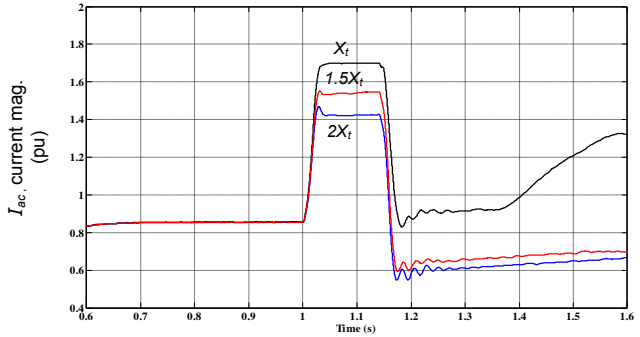


Figure 24.23. *AC converter current for a three-phase fault, with different interfacing inductances.*

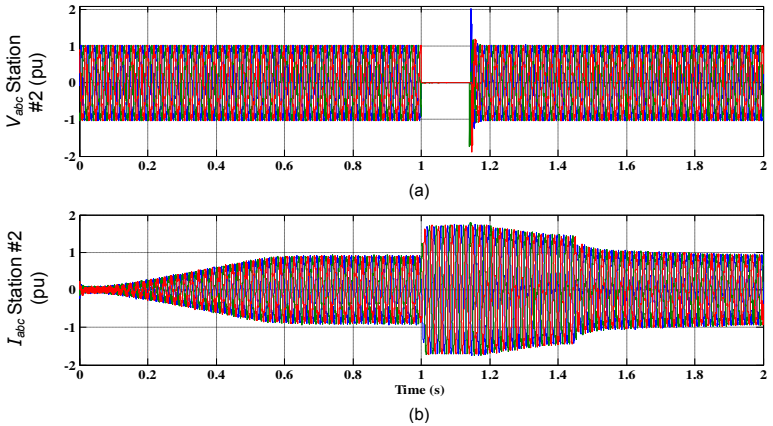


Figure 24.24. *Simulation during ac faults on the inverter grid three-phase ac: (a) voltages and (b) currents.*

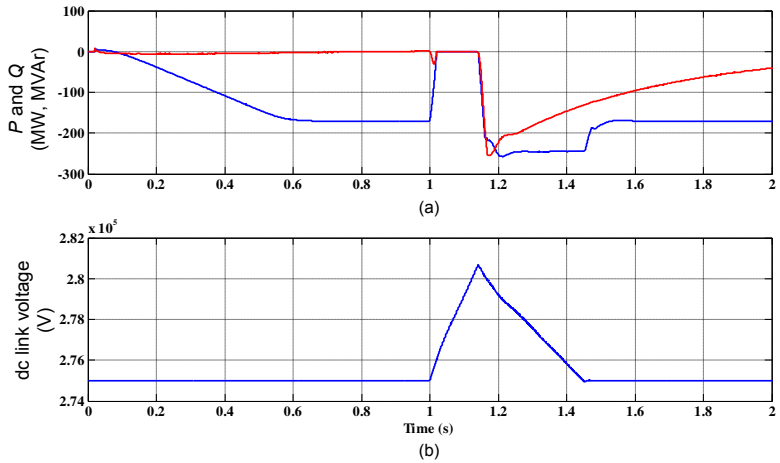


Figure 24.25. *Simulation during ac faults: (a) active and reactive power converter #2 injects into PCC_2 and (b) dc link voltage.*

24.5.2 DC fault - on the dc link

Figure 24.26 shows the VSC test system simulated with short circuit faults, when using a two-level PWM controlled inverter. Figure 24.26 shows the dc fault current path in the inverter diodes acting as a rectifier. During a dc fault, the VSC behaves like an uncontrolled three phase rectifier. Therefore the positive dc rail diode connected to the most positive ac line (D_1, D_3 and D_5) will experience high fault level currents and current returns through the negative rail diode (D_2, D_4 and D_6) connected to most negative ac voltage line. A number of fault paths are created during a dc side fault.

- The first stage of a dc link fault involves the dc link and cable capacitances discharging into the fault.
- When the link capacitance has discharged, the link inductive energy in L_d freewheels through the link fault and the three-phase bridge freewheel diodes (forming three parallel freewheel paths).
- Then the ac current builds up through L_t+L_g, and the rectified current attempts to source the dc fault, until the fault is cleared.
- On recovery the dc link capacitor (and cable capacitance) is charged by inrush current controlled by the ac side inductance, from the ac side through the uncontrolled three-phase bridge diodes.

The exact sequencing and current magnitudes depend on factors like the dc fault location, the dc link and ac side inductances, and the dc link and cable capacitances.

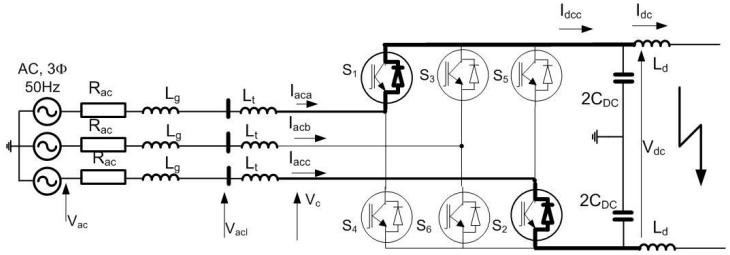


Figure 24.26. *Fault current path through one branch of a VSC for a positive half-cycle.*

During *ac side faults*, both IGBT and diode currents rapidly increase. IGBTs normally have hard-wired local over-current protection, implemented at the gate drive level (mounted on the switch) capable of gate commutating the IGBT within a few microseconds. This type of local current measurement protection is inaccurate, noise prone, and indiscriminate.
During a *dc side fault*, any conducting IGBTs self-commutates, as the diodes take up the fault current from the ac side, which the diodes cannot control. The diode currents track the ac fault current waveforms, which have asymmetrical and symmetrical components. The dc link capacitor discharges simultaneously into the dc fault, controlled by any interposed link inductance.

The symmetrical component of the ac side fault current is the steady-state component, which is:

$$I_{acf} = \frac{V_g}{|z_{ac} + jX_t|} \tag{24.47}$$

where V_g is the grid ac voltage, z_{ac} is the ac impedance, and X_t is the transformer and the ac-side inductor reactance.

The steady-state dc fault current, from the ac side, is the sum of the positive rail (or negative rail) diode currents, namely:

$$I_{dcf} = \frac{\pi}{\sqrt{6}} I_{acf} \tag{24.48}$$

In addition to the symmetrical dc fault component, there is a transient asymmetrical component which depends on the fault instant during the fundamental cycle and the *X/R* ratio. This transient component can cause the first peak to be twice the steady-state fault current. The worst case peak diode current is:

$$I_{acfpm} = \frac{2\sqrt{2}\,V_g}{|z_{ac} + jX_t|} \tag{24.49}$$

The trade off between IGBT and diode die areas within the module package deemed suitable for normal inverter operation, may not favour robustness during dc side faults, when maximising diode die area dominates trade off design.

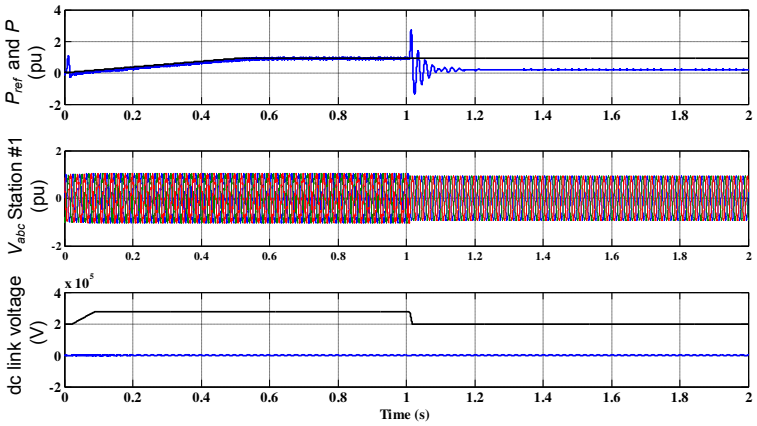


Figure 24.27. *DC fault simulation.*

The test network is subjected to a 140ms solid pole-to-pole dc side fault at the location indicated in figure 24.26. During the dc side fault period, active power exchange between the two grids G_1 and G_2 is interrupted. During system recovery from the temporary dc fault, the link capacitors experience a high inrush charging current, since the power paths between the converter's ac and dc sides are uncontrolled.
The dc fault current is a combination of a grid contribution and from the dc link capacitors. Figure 24.27 shows the results when the test network is subjected to a temporary solid pole-to-pole dc fault at the dc link midpoint.

The challenge faced in the design of all vacuum tube devices is to achieve operating fields in excess of 5 MV/m.
Vacuum voltage related gap mechanisms involve Paschen's law (voltage necessary to start an electric arc between two electrons in a gas as a function of pressure and gap length) and Townsend discharge for a self-sustaining characteristic. Performance is ultimately limited by the presence of electron pin-holes in electrode surfaces, that is, microscopic sites from which electrons can escape from the metal into the vacuum gap by a complex field emission mechanism under anomalously low field conditions. These electronic defects manifest themselves in two ways. First, they give rise to dark leakage or pre-breakdown currents. Second, they trigger the catastrophic "nightmare" phenomenon of vacuum breakdown, that is, the insulating properties of the vacuum gap are spontaneously lost as the result of an electrical discharge between the electrodes (field emission from the cathode).
With typical actuator gap opening speeds are 1mm/ms, a dc disconnector for a hybrid (mechanical plus shunt semiconductor) arrangement requires tens of millisecond to achieve a vacuum gap (of many centimetres) that could standoff hundreds of kilovolts. The shunting semiconductors in the hybrid DCCB would have to survive significantly greater than 10 times nominal current for tens of milliseconds, in a typical ±400kV system, even with an ac side leakage inductance of 0.3pu. This implies the only viable dc circuit breaker solution is a complete fully rated semiconductor solution, in the break path which is the system principle dc current path.

24.5.3 Converter modelling for reduced dc voltage

This section examines converter variables during reduced dc voltage, that is, during a dc fault. Under such depressed dc voltages the VSC controller may saturate, which implies that converter control is lost. In this case, the assumptions of constant dc current or dc voltage, and that the converter provides a direct link between the ac and dc sides according to electrical circuit rules, are no longer valid. This implies that the ac grid be modelled in detail in order to accurately predict the dc current flow.

Assuming the ac grid is represented as an impedance z_{ac} with a series equivalent ac source V_{ac}, the ac current equation is:

$$\bar{I}_{ac} = \frac{\bar{V}_c - \bar{V}_g}{\bar{z}_{ac}} \tag{24.50}$$

where V_c is the converter ac voltage. Expanded equation (24.50) gives:

$$(I_{acd}+jI_{acq})(z_{acd}+jz_{acq})=V_{cd}+jV_{cq}-V_{gm} \tag{24.51}$$

Assuming the converter line-neutral voltages can be expressed in terms of the control signals M_{cd} and M_{cq}:

$$\bar{V}_c=\frac{1}{2\sqrt{2}}\bar{M}_c\,V_{dc}=\frac{1}{2\sqrt{2}}M_{cd}V_{dc}+j\frac{1}{2\sqrt{2}}M_{cq}V_{dc} \tag{24.52}$$

This gives:

$$\begin{bmatrix}I_{acd}\\ I_{acq}\end{bmatrix}=\begin{bmatrix}z_{acd} & -z_{acq}\\ z_{acq} & z_{acd}\end{bmatrix}^{-1}\begin{bmatrix}\frac{1}{2\sqrt{2}}M_{cd}V_{dc}-V_{gm}\\ \frac{1}{2\sqrt{2}}M_{cq}V_{dc}\end{bmatrix} \tag{24.53}$$

that is

$$\begin{bmatrix}M_{cd}\\ M_{cq}\end{bmatrix}=\left\{\begin{bmatrix}V_{gm}\\ 0\end{bmatrix}+\begin{bmatrix}z_{acd} & -z_{acq}\\ z_{acq} & z_{acd}\end{bmatrix}\begin{bmatrix}I_{acd}\\ I_{acq}\end{bmatrix}\right\}\frac{2\sqrt{2}}{V_{dc}} \tag{24.54}$$

Assuming I_{acd} and I_{acq} are controlled at their reference values, equation (24.54) can be used to determine M_{cd} and M_{cq} for each V_{dc} value. As V_{dc} reduces, the control signals saturate, where $M_{cd}=1$, $M_{cd}=1$ and the converter loses control. Figure 24.28 shows the controller structure. When the converter saturates, the currents increase as the dc voltage reduces according to equation (24.53).
The dc current when the VSC is active can be calculated from the VSC power balance equation:

$$\sqrt{\frac{2}{3}}\left(V_{cd}I_{acd}+V_{cq}I_{acq}\right)=V_{dc}I_{DC} \tag{24.55}$$

Therefore using equations (24.52) and (24.55), the dc current is:

$$I_{DC}=\frac{1}{2\sqrt{3}}\begin{bmatrix}M_{cd} & M_{cq}\end{bmatrix}\begin{bmatrix}I_{acd}\\ I_{acq}\end{bmatrix} \tag{24.56}$$

Then by substituting I_{acd} and I_{acq} from (24.53), the dc current can be calculated.

The magnitude of ac currents I_{acd} and I_{acq} reflects the magnitude of the instantaneous currents through the switches. Therefore the magnitude of the ac currents is controlled. If high currents are detected, the controller inhibits the IGBT switches and the VSC becomes an uncontrolled three-phase diode rectifier bridge.

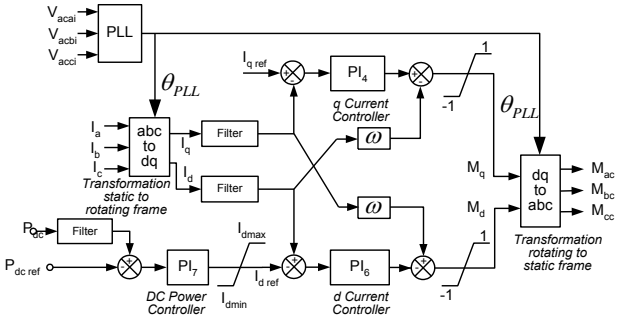


Figure 24.28. *VSC controller structure.*

Diodes usually have high over-current capability and can feed a dc fault for milliseconds. An uncontrolled diode bridge operates as a 6-pulse converter and the magnitude of the ac voltage (*L-N*) as a function of dc voltage is:

$$\bar{V}_{acdb}=\frac{1}{\sqrt{2}}\frac{\pi}{3}V_{dc} \tag{24.57}$$

This ac voltage is substantially different from the VSC ac voltage in equation (24.52). Consequently there is a high current surge I_{DC} when the IGBT switches are inhibited. Using equation (24.50), the current I_{acdb} for the diode bridge is

$$I_{acdbm}e^{j\theta Idb}=\frac{V_g e^{j0}-V_{acdbm}e^{j\theta Vdb}}{z_{ac}e^{j\theta z}} \tag{24.58}$$

or expanded into magnitude and angle components:

$$I_{acdbm}=\frac{\sqrt{\left(V_g-V_{acdbd}\right)^2+V_{acdbd}^2}}{z_{acm}}$$
$$\theta_{Idb}=-\theta_{Vdb}-\theta_z \tag{24.59}$$

where I_{acdbm} is the ac current magnitude and θ_{Idb} is the angle of the current in the diode bridge. The angle θ_{Vdb} is the voltage angle and θ_z is the ac impedance angle. The current in a diode bridge will slightly lag the ac voltage:

$$\theta_{Idb}=\theta_{Vdb}-\theta_\gamma \tag{24.60}$$

where the power factor angle for a diode bridge θ_γ is:

$$\cos\theta_\gamma=1-\frac{3X_{ac}}{\pi}\frac{I_{DC}}{V_{dc}} \tag{24.61}$$

This power factor angle is small, 5° to 10°, but can be large for a low dc voltage and high dc current. Therefore using (24.59) and (24.60), the ac voltage angle for a diode bridge is:

$$\theta_{Vdb}=½\left(-\theta_z+\theta_\gamma\right) \tag{24.62}$$

Substituting equation (24.62) into (24.59) gives the current magnitude:

$$I_{acdbm}=\frac{\sqrt{\left(V_{gm}-\frac{1}{\sqrt{2}}\frac{\pi}{3}V_{dc}\cos\theta_{Vdb}\right)^2+\left(\frac{1}{\sqrt{2}}\frac{\pi}{3}V_{dc}\sin\theta_{Vdb}\right)^2}}{z_{acm}} \tag{24.63}$$

This equation gives the fault current magnitude dependence on the dc voltage. The diode bridge dc current is linked to the ac current magnitude by:

$$I_{dcdb}=\frac{\pi}{\sqrt{6}}I_{acdbm} \tag{24.64}$$

Therefore equations (24.63) and (24.64) give the dc current as a function of the dc voltage:

$$I_{dcdb}=\frac{\pi}{\sqrt{6}}\frac{1}{z_{acm}}\sqrt{\left(V_{gm}-\sqrt{\frac{3}{2}}\frac{\pi}{3}V_{dc}\cos\frac{-\theta_z+\theta_\gamma}{2}\right)^2+\left(\sqrt{\frac{3}{2}}\frac{\pi}{3}V_{dc}\sin\frac{-\theta_z+\theta_\gamma}{2}\right)^2} \tag{24.65}$$

This equation is nonlinear and can be solved iteratively since θ_γ is a function of V_{dc} in (24.61). However, the term θ_γ has minimal impact on the fault current, while the impact of the magnitude of the ac impedance z_{acm} is significant. Therefore it is assumed that θ_γ is constant and is calculated for nominal conditions. Now equation (24.65) can be linearized. Figure 24.29 shows the dc current as a function of dc voltage for a VSC and a diode bridge.

The following operating regions are shown:

- Ⓐ-Ⓑ normal operation. The controller regulates the dc current at rated value.
- Ⓑ-Ⓒ the controller saturates. I_d and I_q are increasingly uncontrollable as V_{dc} reduces
- Ⓒ-Ⓓ the IGBTs are tripped and the VSC becomes an uncontrollable diode rectifier bridge.
- Ⓓ-Ⓔ the converter operates as a diode rectifier bridge: dc current increases as dc voltage reduces.

Generally VSC based hvdc controllers use sinusoidal modulation ($M\leq1$) in both power flow directions, in order to avoid common voltages. Enhance dc fault control can be achieved by using triplen injection ($M\leq1.155$). Although common to dc to ac conversion in order for better dc link utilisation, triplen injection in an ac to dc converter allows dc link control below the uncontrolled rectifier voltage level, down to 0.866pu. Lower dc fault levels result. In order to avoid common mode voltage effects, the system configuration and filtering may dictate that triplen injection only be employed during dc fault conditions.

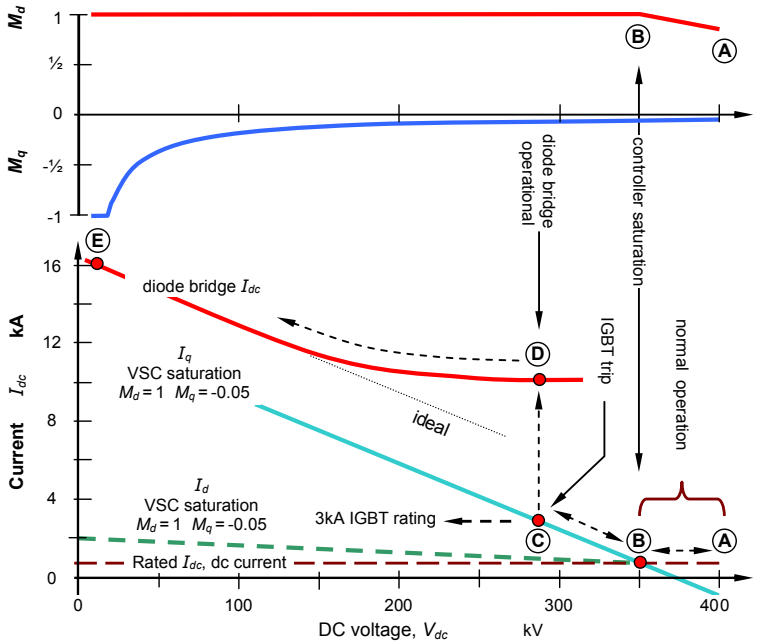


Figure 24.29. *VSC mode transitions as the dc link voltage reduces during dc fault.*

24.5.4 Influence of the dc link capacitors

In general, the dc link shunt capacitors increase the fault current but the capacitors are typically discharged in a short time interval at the beginning of a dc fault. The magnitude of the initial capacitor fault current is only limited by the impedance in the fault path (cable impedance) and damping resistors if they are installed in the capacitor banks. In the case of longer fault clearing times, the capacitors impact on the overall fault energy.

The main issue with dc capacitors is the initial peak current. A solution is to use dc side inductors. These inductors limit the capacitor discharge current and also limit the transient increase of the main dc fault current from the ac grid. The presumption with this protection method is that there will never be a dc fault between the converter and the inductors.

24.6 VSC HVDC interaction with ac systems

24.6.1 Power flow between ac systems

With VSC PWM control, the phase angle and voltage amplitude (within limits set by the dc link voltage magnitude) can be controlled by changing the SPWM modulation depth and the relative phase displacement respectively, as in figure 24.30. A phase locked loop is used to grid synchronise the displacement, which facilitates independent control of the active and reactive powers.

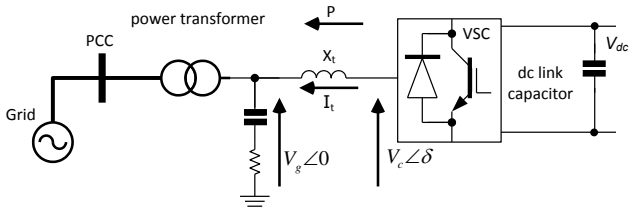


Figure 24.30. *A grid connected VSC.*

The VSC bridge can be viewed as a controllable synchronous machine but with a fast dynamic response having an instantaneous output phase voltage of

$$V_c = ½ V_{dc} M \sin(\theta + \delta) + Harmonics \tag{24.66}$$

where M is the modulation index and δ is the output voltage phase shift. These two variables can be adjusted independently to obtain any combination of voltage amplitude and phase shift in relation to the fundamental frequency voltage of the ac system. This controls the active and reactive power flows.

The power flow between the two ac sources, V_g and V_c in figure 24.30, can be analysed by considering two networks or a generator and a network. Such a system represents a VSC-HVDC connected to a power grid. The interfacing filter is represented as a purely inductive L-filter, where for expedience, the inductor's resistive element is ignored.

This power exchange situation has been considered in Chapter 25, but a different analysis approach is presented here, but with the same result.

The complex S, active P, and reactive Q powers exchanged by the source V_c are:

$$\begin{gathered} S = \bar{V}_c \, \bar{I}_t^* \\ P = \mathrm{Re}(\bar{S}) = \mathrm{Re}(\bar{V}_c \, \bar{I}_t^*) \qquad Q = \mathrm{Im}(\bar{S}) = \mathrm{Im}(\bar{V}_c \, \bar{I}_t^*) \end{gathered} \tag{24.67}$$

The current is:

$$\begin{aligned} \bar{I}_t &= \frac{\bar{V}_c - \bar{V}_g}{jX_t} = \frac{V_c\angle\delta - V_g\angle 0}{jX_t} \\ &= \frac{V_c\angle(\delta - ½\pi) - V_g\angle -½\pi}{X_t} \end{aligned} \tag{24.68}$$

Separating (24.68) into real and imaginary components:

$$\begin{aligned} \bar{I}_t &= -\frac{V_c}{X_t}\cos(\delta - ½\pi) + j\left[\frac{V_g}{X_t} + \frac{V_c}{X_t}\sin(\delta - ½\pi)\right] \\ &= \frac{V_c}{X_t}\sin\delta + j\left[\frac{V_g}{X_t} - \frac{V_c}{X_t}\cos\delta\right] \end{aligned} \tag{24.69}$$

Using (24.67), the complex power is:

$$\bar{S} = \bar{V}_c \, \bar{I}_t^* = \frac{V_c V_g}{X_t}\sin\delta + j\left[\frac{V_c V_g}{X_t} - \frac{V_c V_g}{X_t}\cos\delta\right] \tag{24.70}$$

Substituting this equation into the equations in (24.67):

$$P = \frac{V_c V_g}{X_t}\sin\delta \qquad Q = \frac{V_c^2}{X_t} - \frac{V_c V_g}{X_t}\cos\delta \tag{24.71}$$

These power equations for P and Q enable the study of active and reactive power exchange between two ac systems. The power P equation in (24.71) represents active power exchange and is graphically represented in figure 24.31, where the power curves $P(X_t)$ correspond to two different interfacing reactors. There is no power exchange if the two voltages have the same angle (δ=0), regardless of the voltage magnitudes, since the resultant current is at quadrature to the voltages. Maximum power transfer is achieved if the angle between the two voltages is ½π. The system is unstable with angles above ½π, and therefore in practice the angle between the networks is maintained below ½π. Also increased interfacing reactance reduces the power transfer as shown in figure 24.31. In transmission systems, the voltages are near equal, therefore the active power flow is dominated by the angle between the networks, and the tie-line impedance.

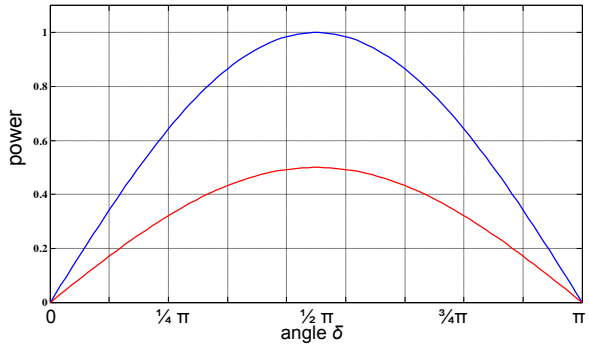


Figure 24.31. *Active power transfer curve for a two ac-source system.*

24.6.2 Operation with a passive ac system

A HVDC VSC can provide black start capability, assuming dc link voltage is available. The converter ac voltage can be readily shaped by the controller, thus a VSC can be made to appear as a synchronous machine to the ac grid. The converter ac voltage can be regulated from low values and the converter ac frequency can also be internally set for the period before the system large generators establish normal operation.

If a converter supplies a passive ac grid, as shown in figure 24.32, the main control mode will be ac system frequency control. The converter provides the required active power in order to keep the system frequency at a set value. A PI controller adjusts the converter power until the output frequency matches the set value. The *q*-control loop is configured to control the ac voltage.

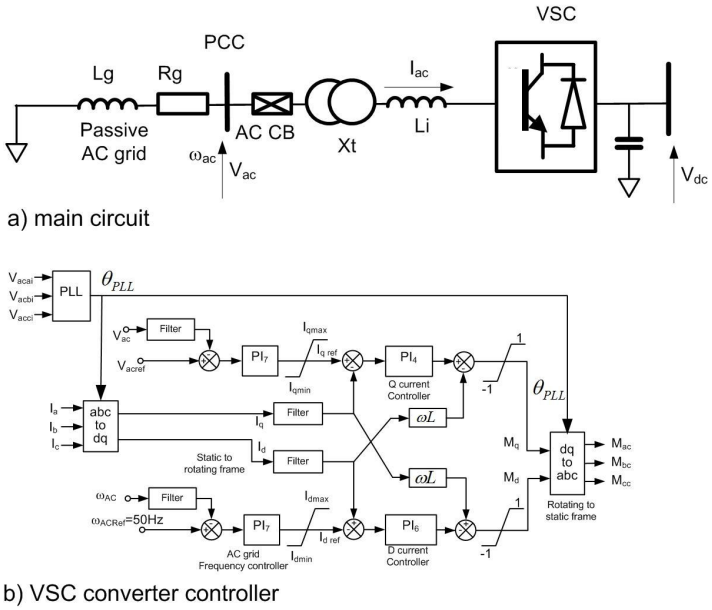


Figure 24.32. *HVDC VSC connected to a passive ac grid.*

24.7 HVDC VSC harmonics and filtering

Voltage sourced converters generate harmonics on both the ac and dc sides due to converter switching action. For VSC-HVDC integration, the amplitude of the harmonics entering the ac network and the dc line are limited, in accordance with harmonics standards. Different techniques are used to reduce the harmonics to within limits, such as:

- pulse width modulation (PWM) and selective harmonic elimination SHE techniques
- multi-pulse topologies
- multi-level topologies
- harmonic filters
- combinations of these

24.7.1 Converter modulation

Various modulation strategies are presented in chapter 17.
PWM is the dominant modulation technology use in VSC-HVDC systems, due to the simple power circuit and low complexity control strategies. The most common PWM techniques used in VSC-HVDC are:

- sinusoidal carrier based modulation, SPWM
- selective harmonic elimination (SHE) modulation,

Space vector modulation, SVM, is not employed since it assumes three symmetrical ac phases.
Figure 24.33 shows the PWM VSC control signals (intersection of triangular carrier signal and sinusoidal reference voltages), where the carrier frequency (triangular wave signal) is nine times the fundamental output frequency.

The switching angles α_0, α_1, α_2, α_M, π are used by the controller as the gating signals to the IGBT switches. There are $2M$+1 switching instants per half cycle. The amplitudes of the harmonics of the output waveform are given by:

$$V_n = \frac{2V_{dc}}{n\pi}\left(1+\sum_{k=1}^{2M}(-1)^k \cos n\alpha_k\right) \tag{24.72}$$

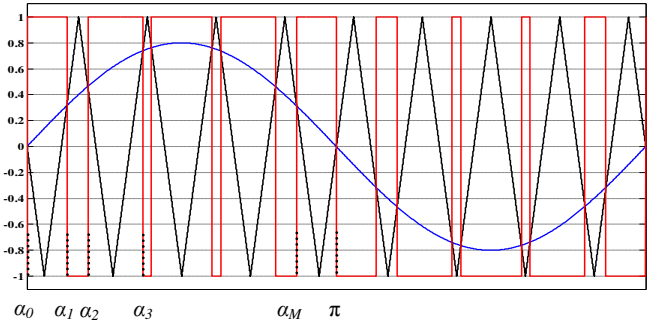


Figure 24.33. *VSC SPWM and output voltage.*

If the triangular carrier signal frequency is an odd integer multiple of the fundamental frequency, the waveform does not contain even order harmonics. In a three-phase bridge circuit, all the triplen harmonics, that is, the 3rd, 9th … are eliminated from the line voltages, provided the ac system voltages are balanced and harmonic distortion free. Also, if the triangular signal frequency is a multiple of 3 times the fundamental, the harmonics of the order of the triangular signal frequency cancel in the line and phase to floating neutral voltages.
The harmonic spectrum of the inverter output voltage is affected by the modulation technique employed. In the case of six step modulation, the harmonic spectrum can be obtained using Fourier analysis. The signal is time in-variant and periodic.
Being non-periodic in nature, the PWM modulation harmonic analysis case is more complex. The waveform can be described as a two variable function where the carrier and the reference waveforms periodically across. The PWM waveform harmonics can be expressed in a general form as a double summation Fourier series:

$$F(t) = \tfrac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_0 t + B_{0n}\sin n\omega_0 t) + \sum_{m=1}^{\infty}(A_{m0}\cos n\omega_c t + B_{m0}\sin n\omega_c t) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}(A_{mn}\cos(m\omega_c + n\omega_0)t + B_{mn}\sin(m\omega_c + n\omega_0)t) \tag{24.73}$$

The coefficients of (24.73) can be obtained for any particular PWM strategy by evaluating the following double Fourier integral:

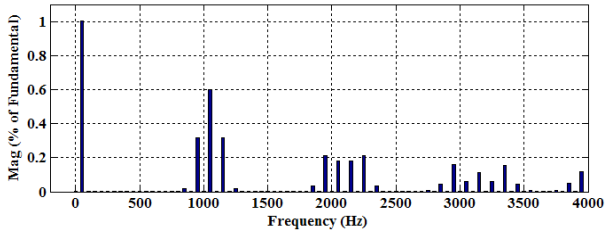
$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} F(x,y)e^{j(mx+ny)}dxdy \tag{24.74}$$

where $x = \omega_c t$ and $y = \omega_o t$.

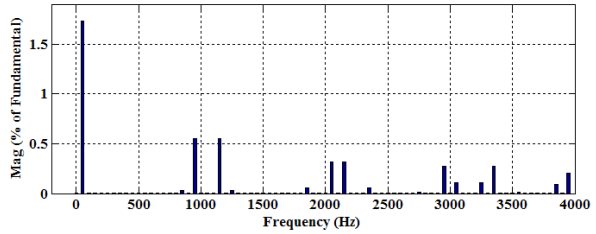
The inverter output harmonics can be classified as:

- low frequency harmonics (baseband harmonics);
- switching frequency harmonics (carrier harmonics); and
- high frequency harmonics (sideband harmonics).

Typical output phase to floating neutral voltage and line voltage spectra are shown in figure 24.34 parts a and b with total harmonic distortion, THD, of 68%, and 99%, respectively. The carrier frequency is 1050 Hz; 21 times the fundamental frequency (that is, 21 (=7x3) is an odd integer multiple and divisible by 3).



(a)



(b)

Figure 24.34. *Spectra analysis:*
(a) phase to floating neutral voltage spectrum and (b) line voltage spectrum.

24.7.2 Multi-pulse and multilevel converters

Techniques to reduce output harmonics use multi-pulse and multilevel converter topologies.
Multi-level converters are presented chapter 17. The stepped output ac wave can be more sinusoidal by increasing the number of step levels. The output waveform harmonics are calculated by Fourier analysis.

Series connection of phase shifted converters, can eliminate specific harmonics both on the dc and ac sides. Figure 24.35 shows a 12-pulse VSC, where the 30° phase shift is achieved by the use of a star and delta transformer secondary configuration.

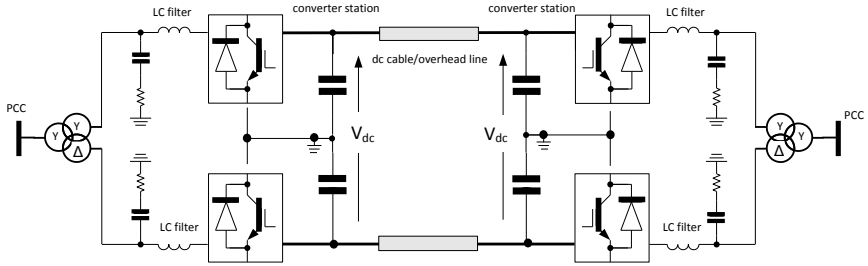


Figure 24.35. *HVDC-VSC using a twelve-pulse Y/Δ transformer secondary arrangement.*

24.7.3 Comparison of harmonic content at the ac terminals

VSCs can be characterised according to number of levels and the type of modulation. Table 24.1 shows typical total harmonic distortion, THD, at the output of different VSC-HVDC topologies, before any passive filtering, where SPWM is used in each case.

Table 24.1. Output voltage THD for different VSC topologies.

Level	Converter topology	THD
2	2-level 6-pulse converter	60%
3	3-level 12-pulse converter	30%
4	4-level 6-pulse converter 3-level 12-pulse converter	20%
5	5-level 6-pulse converter	15%

The passive filtering must decrease the harmonics, depending on the ac voltage level, according to standard IEEE-519, as indicated in Table 24.2.

Table 24.2: Voltage distortion limits according to IEEE-519 standard.

Bus Voltage at Point of Common Coupling PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
below 69kV	3	5
69kV to 137.9kV	1.5	2.5
138kV and above	1	1.5