CHAPTER 12

Device Protection

This chapter considers various areas of power device application that are often overlooked, or at best, underestimated. Such areas include over-current, overvoltage and short circuit protection.

12.1 Protection overview - over-voltage and over-current

All electrical systems are vulnerable to interference and damage from lightning or other short duration electrical surges or long duration supply system swells. As systems become more electronically complex, they also become more vulnerable to external and internally generated interference. A fault can be caused by a device failure or noise which results in undesired device turn-on. This will cause semiconductor device and equipment failure unless protective measures are utilised.

Protection against fault current effects usually involves fuses which clear in time to protect endangered devices, or voltage transient absorption devices which absorb spike energy and clamp the equipment voltage to a safe level. The crowbar fault protection technique can be employed to divert the fault from sensitive components to the crowbar which is a robust circuit. The crowbar clamps the sensitive circuit to zero volts and initiates an isolation breaker or fuse action.

An electrical surge is a temporary increase in voltage, current or both. The size, waveform, and form of the transient surge which can occur within a system are many and varied.

i. Lightning - Although direct strike lightning current can potentially generate transients in the millions of volts and tens of thousands of amps, electronic equipment is rarely exposed to surges of this magnitude. The greatest exposure in power electronics systems is through interconnection and transmission lines. Domestic ac lines can only carry voltages up to 5kV and currents of the order of 1kA. Therefore, for the vast majority of instances where the chance of a lightning strike directly to the equipment is low, 5kV and 1kA is the limit of the direct strike or inductively generated surges. Exposed equipment, such as wind turbines, although suitable earthed, can experience significantly higher electrical surge stresses.

ii. Power Induction - Although power induction voltages can be high in voltage and current, they are often limited in duration. These voltages are caused by faults on the power system which couple into the system (usually inductively as a consequence of the surge causing a large fault current). In power transmission systems, these faults are quickly terminated by circuit breaker and re-closer equipment. This can occur in as short as a couple of cycles of power frequency voltage and rarely takes longer than a second. These transients are typically modelled as a 600Vrms waveform lasting up to a second.

iii. Power Cross - Alternatively, power cross voltages are low voltage events but the exposure can occur for long durations. They are often caused by maintenance error or cabling faults and can result in moderate currents flowing for a long period of time, for example, in domestic applications, 25A for 15 minutes. They are predominately at mains power supply voltage levels (100 to 220Vrms).

iv. Earth Potential Rise (EPR) - EPR can be categorized into two forms:

1. as a result of power system faults and
2. lightning discharges.

In normal industry, where fault currents from the power system are limited in magnitude by fuses and circuit breakers, power system EPR is not usually a considerable risk. EPR only becomes a significant risk when power earthing systems are significantly below standard or where high power transmission systems are used such as at power generation and distribution facilities, within the high power industry, and in the vicinity of electrical traction systems (electric rail). Lightning EPR can only result from a direct strike to the building housing the equipment or in its immediate vicinity. Such events are uncommon, unless the installation is particularly vulnerable due to location or extreme height (for example, wind turbine and cellular phone base-station antennae). The equipment exposure as a result of EPR can be high, and at high earth resistance locations, may become a significant portion of the lightning current.

Surge protection is the process of protecting electronic systems or equipment from voltages and currents which are outside their safe operating limits. These surge voltages and currents can be generated by short circuits, lightning or faults from a power system and usually enter the electronic system along inter-equipment wiring. The surges may be galvanically coupled into the system as in the case of a direct lightning strike, through an inadvertent connection of the power system to the wiring, or as a result of an earth potential rise. They may be capacitively coupled into the system which may occur when a data system is used in the vicinity of a high voltage power line. They may be inductively coupled into the system as may occur if the wiring is run in parallel with large currents running in a power circuit feeding a high power motor. Such events can result in a wide variety of potential consequences.

Electrical surge protection performs several key functions:

- it must prevent or minimize damage caused by a surge;
- it must ensure the system returns to a working condition with minimal disruption to service.
- under normal conditions the protection must not interfere with any signals or control circuitry, creating challenges for power electronics technologies.
- the protection must operate and fail in a safe predictable manner during overstress.

12.1.1 Ideal secondary level protection

Power electronic equipment is generally within a system that has primary protection, associated with the ac grid protection, for example. The installed equipment therefore may only require secondary protection. Secondary protection prevents the let-through energy of the primary protector (the energy of the surge which gets past the primary protector) from damaging the load.
The peak open circuit voltage of the let-through energy past the primary protector is smaller than the initial external surge. Therefore, a secondary protector can effectively block (series) and or divert (shunt) the reduced surge energy.
The requirements for this ideal blocking device are:

i. As the device needs to block the let-through energy of the primary protector, it can be a series component (in series with the transmission line), located just after the primary protector. As a series component, the device will react to the current through the device rather than, as with a shunt protector, voltage across the interface.

ii. A series device should have a predictable, stable and low trigger current (current at which the device changes between its conductive and non-conductive state) to provide effective protection for sensitive downstream equipment. A shunt device should operate (clamp or fold-back) at a level just above the maximum working voltage (but below device failure level).

iii. It should be fast acting (less than 10ns) to protect equipment from surges which rise at 5kV/μs - as with direct lightning strikes or lightning EPR;

iv. As a series device it should have low impedance (resistive, capacitive and inductive) so that it does not effect normal circuit operation, while for the same reasons, a shunt device should have a high standby impedance;

v. In the blocking mode, a series protector should have high impedance so that it does not dissipate significant energy during long duration surges, while for the same reasons, a shunt device should have a low clamping impedance;

vi. It should reset after the surge to reinstate the system and continue to allow normal operation;

vii. Reset to normal after an incident, returning the equipment to pre-event operation;

viii. Debatably, after excessive stress, a shunt device should fail-safe open circuit, while a series device should failure short-circuit, so as to enable continued unprotected operation, but system protection is afforded.

In addition, for practical and economic reasons it should be small in size, light in weight, and low in cost.

Electrical protection devices fall into two key categories: overvoltage (usually shunt connected) and over-current (usually series connected). Over-voltage devices divert or shunt surge current produced by an over-voltage (such as lightning), as shown in Figure 12.1, while most over-current devices increase in resistance (possibly becoming open-circuit) to limit the surge current flowing from longer duration surge currents (50/60 Hz power fault), as shown in the parts of figures 12.2.

There are two types of voltage limiting protectors: switching devices (gas discharge tube GDT and thyristor) that crowbar (voltage fold-back) the line, and voltage clamping devices (metal oxide varistor MOV and transient voltage suppressor TVS). The waveforms of figure 12.1 highlight that switching devices result in lower stress levels than clamping devices (shaded area) for protected equipment during their operation. Functionally, all voltage protectors reset after the surge, while current protectors may or may not reset, depending on their operating mechanisms. For example, PTC thermistors are resettable; fuses are non-resettable.

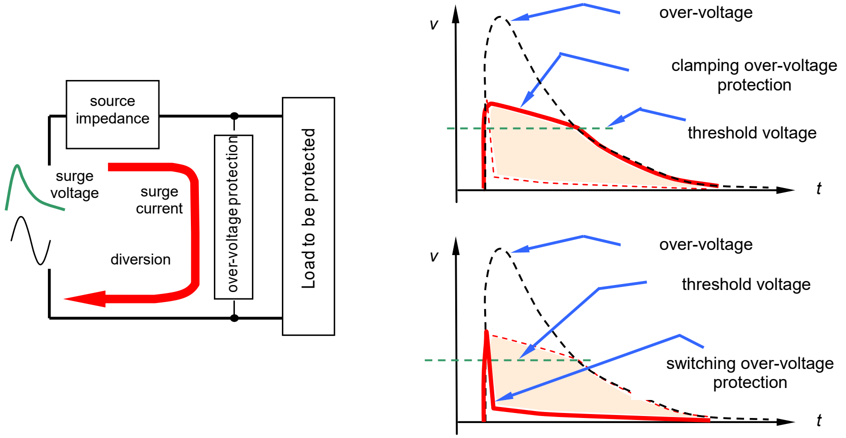

Figure 12.1. *Two shunt voltage control mechanisms, namely voltage clamping and voltage fold-back by switching action, with source and load voltages shown.*

12.1.2 Overvoltage protection devices

Gas Discharge Tubes (GDT) create a quasi short circuit across the line when the internal gas is ionized by an overvoltage, returning to a high impedance state after the surge has ceased. These robust devices have the highest impulse current capability of any technology, and combined with negligible capacitance, make them attractive for the protection of high-speed digital and ac switching converter applications.

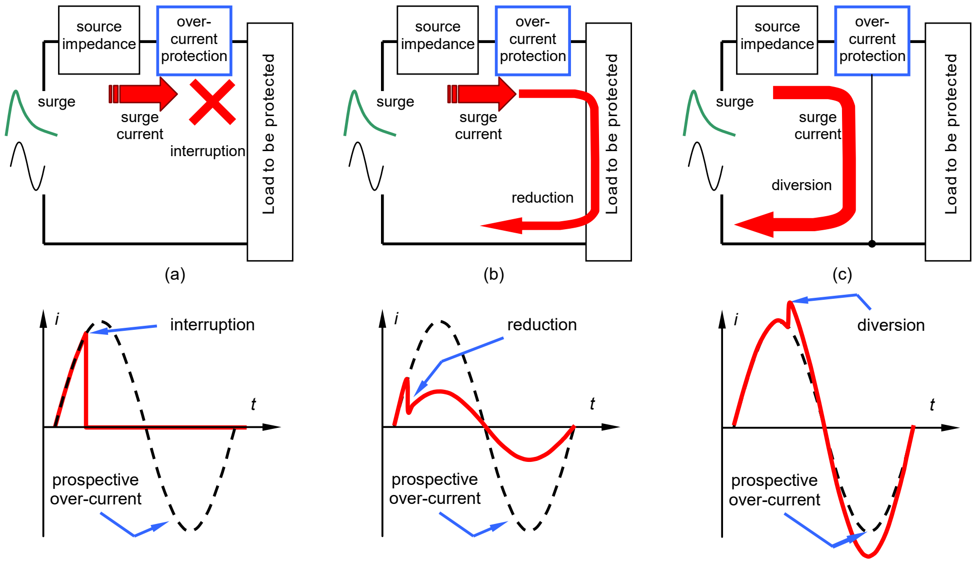

Figure 12.2. *Three current limiting mechanisms:*
(a) current flow interruption, (b) current reduction, and (c) current diversion.

Thyristor-based devices initially clamp the line voltage, and then switch to a low voltage on-state. After the surge, when the current drops below the holding current, the protector recovers and returns to its original high impedance blocking state.
Transient Voltage Suppressor (TVS) or Zener diodes operate by rapidly moving from a high impedance to a non-linear resistance characteristic that clamps surge voltages. TVS diodes provide a fast-acting and controlled clamping voltage, however they have high capacitance and low energy capability which restricts the maximum surge current.
Electrostatic discharge (ESD) devices clamping protectors consists of multilayer varistors (MLV) designed to protect equipment against ESD conditions. They have low leakage currents that make the devices transparent under normal operation. ESD transients cause the device to clamp the voltage by reducing its effective resistance and it resets to a high impedance state after the disturbance. Diode arrays for ESD protection combine thin film on silicon wafer fabrication technology and chip scale packaging. Such devices are used in portable electronics applications where a particular electrical response characteristic is specified for a minimum volume.

12.1.3 Over-current protection devices

Polymer Positive Temperature Coefficient (PPTC) Thermistor resettable fuses are used in circuit current protection applications. Under high-current fault conditions, its resistance increases by many orders of magnitude and remains in a tripped state, continuing to provide continuous circuit protection until the fault is removed. Then after the power is cycled, the device returns to its normal low-resistance, low-loss state.
Traditional fuses are constructed from a metal element encapsulated in a ceramic housing. The fuse element heats up at the rate related to I^2R. When the metal element temperature exceeds its melting point, it vaporizes and opens the circuit. The low resistance and losses of fuses are attractive for ac applications.
Line Protection Modules (LPM) are based on a basic form of current protection; the Line Feed Resistor (LFR), normally fabricated as a thick-film resistor on a ceramic substrate. LPMs can withstand high-voltage impulses without breaking down. AC current interruption results when the high temperature developed by the resistor produces mechanical expansion stresses that cause the ceramic to break open. This capability is exploited in modules incorporating both over-current and over-voltage devices on one ceramic substrate. The incorporation of silicon die and discrete components gives modules with high performance and specific functionality.

A concise overview of generally available over-voltage and over-current protection devices is presented in Table 12.1. The following sections will consider each technology in detail.

Table 12.1: Overview of over-current and over-voltage protection devices and technologies

Device	action	connection	speed	accuracy	current rating
Over-voltage					
GDT	voltage switching	shunt	fair	fair	very high
Thyristor	voltage switching	shunt	fair	good	high
MOV	voltage clamping	shunt	fair	poor	high
TVS	voltage clamping	shunt	fast	good	low
Over-current					
Polymer PTC thermistor	resettable	series	fair	good	low
Ceramic PTC thermistor	resettable	series	slow	good	low
Fuse	non-resettable	series	very slow	fair	medium/high
Heat coil	non-resettable	shunt or series	very slow	poor	low
Thermal switch, LFR	non-resettable	series	very slow	poor	high

12.2 Over-current protection

Current limiting devices provide a slow response, and are primarily aimed at protection from surges lasting hundreds of milliseconds or more, including power induction or contact with AC power. By combining a fixed resistor in series with a resettable protector, an optimum balance of nominal resistance and operating time is obtained. The inherent resistance of certain over-current protectors can also be useful in coordination and discrimination between primary and secondary overvoltage protection.

Positive Temperature Coefficient (PTC) Thermistors
Heat generated by current flowing in a PTC thermistor causes a step function increase in resistance towards an open circuit, gradually returning close to its original value once the current drops below a threshold value. The resistance stability after surges over time is a key aspect for preserving line balance. PTCs are commonly referred to as resettable fuses, and since low-level current faults are common, automatically resettable protection can be particularly important.

Fuses
A fuse heats up during surges, and once the temperature of the metallic element exceeds its melting point, the normal low resistance creates an open circuit. The low resistance of fuses is attractive for power applications, but their operation is relatively imprecise and time-dependant. Once operated, they do not reset. Fuses also require additional resistance for primary coordination.
Since overvoltage protection usually consists of establishing a low impedance path across the equipment input, overvoltage protection itself will cause high currents to flow. Although relatively slow acting, fuses play a safety role in removing longer-term faults that would damage protection circuitry, thus reducing the size and cost of other protection elements. It is important to consider the I-t performance of the selected fuse, since even multiples of the rated current may not cause a fuse to rupture except after a significant delay. Coordination of this fuse behaviour with the I-t performance of other protection is critical to ensuring that there is no combination of current-level and duration for which the protection is ineffective. By including structures intended to rupture under excess current conditions or separate components, it is also possible to produce hybrid fusible resistors.

Heat Coils
Heat coils are thermally activated mechanical devices connected in series with the line being protected, which divert current to ground. A series coil operates a parallel shunt contact, typically by melting a solder joint that is restraining a spring-loaded contact. When a current generates enough heat to melt the joint, the spring mechanically forces two contacts together, short-circuiting the line. Heat coils are ideal to protect against 'sneak currents' that are too small to activate other methods. Their high inductance makes them unsuitable for digital lines. It is also possible to construct current interrupting heat coils which open the circuit as a result of over-current.

Line Feed Resistors
A Line Feed Resistor (LFR) is the most fundamental form of current protection, normally fabricated as a thick-film device on a ceramic substrate. With the ability to withstand high voltage impulses without breaking down, AC current interruption occurs when the high temperature developed by the resistor causes mechanical expansion stresses that result in the ceramic breaking open.
Low current power induction may not break open the LFR, creating long-term surface temperatures of more than 300°C. To avoid heat damage to the adjacent components, the maximum surface temperature can be limited to about 250°C by incorporating a series thermal fuse link on the LFR. The link consists of a solder alloy that melts when high temperatures occur for 10 seconds or more periods.
Along with the high precision needed for balanced lines, LFRs have significant flexibility to integrate additional resistors, multiple devices, or even different protection technology within a single component. One possible limitation is the need to dimension the LFR to handle the resistive dissipation under surge conditions. Along with combining multiple non-inductive thick-film resistors on a single substrate to achieve matching to <1%, a resistor can be combined with other devices to optimize their interaction with the overall protection design. For example, a simple resistor is not ideal for protecting a wire, but combining a low value resistor with another over-current protector provides closer protection and less dissipation than either device can offer alone. Both functions can be integrated onto a single thick-film component using fusible elements, PTC thermistors, or thermal fuses. Similarly, more complex hybrids are available, adding surface mount components such as thyristor protectors, to produce coordinated sub-systems.

Thermal Switches
These switches are thermally activated, non-resetting mechanical devices mounted on a voltage-limiting device (normally a GDT). There are three common activation technologies: melting plastic insulator, melting solder pellet or a disconnect device.
Melting occurs as a result of the temperature rise of the voltage-limiting device's thermal overload condition when exposed to a continuous current flow. When the switch operates, it shorts out the voltage-limiting device, typically to ground, conducting the surge current previously flowing through the voltage limiting device.

- A plastic-melting based switch consists of a spring with a plastic insulator that separates the spring contact from the metallic conductors of the voltage limiting device. When the plastic melts, the spring contacts both conductors and shorts out the voltage limiting device.
- A solder-pellet-melting based switch consists of a spring mechanism that separates the line conductor from the ground conductor by a solder pellet. In the event of a thermal overload condition, the solder pellet melts and allows the spring contacts to short the line and ground terminals of the voltage-limiting device.
- A 'snap action' switch typically uses a spring assembly that is held in the open position by a soldered standoff and will short out the voltage-limiting device when its switching temperature is reached. When the soldered connection melts, the switch is released and shorts out the line and ground terminals of the voltage limited device.

12.2.1 Protection with fuses
It is not economical to design a circuit where fault overloads are catered for by using devices and components which will withstand worst-case faults. A fuse link is normally used for circuit fault current protection. A fuse link is a current sensitive device designed to serve as the intentional weak link in the electrical circuit. Its function is to provide protection of discrete components, or of complete circuits, by reliably melting under current overload conditions. A fuse link protecting a semi-conductor is required to carry normal and overload currents but to open the circuit under fault conditions before the semiconductor is damaged. The resultant circuit induced fuse arcing voltage must not cause damage to the circuit. Other fuse links or circuit breakers should be unaffected when the defective cell is disconnected. This non-interaction property is termed *discrimination.*

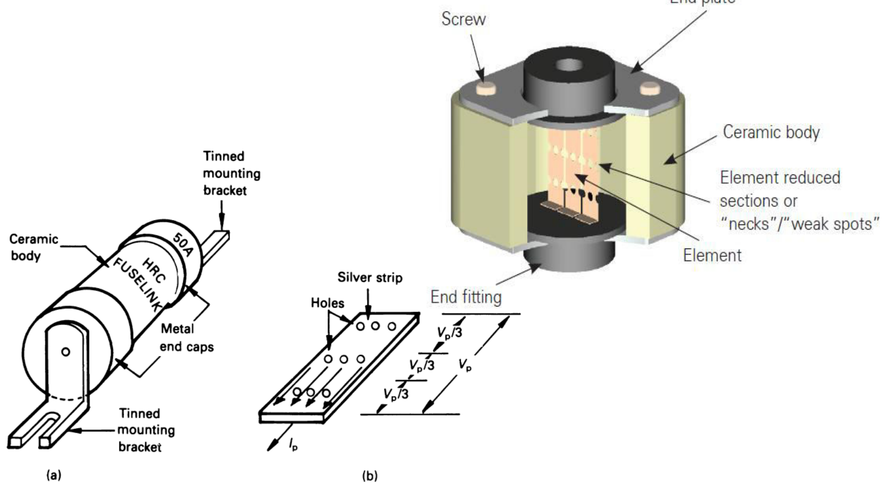

Figure 12.3. *The current fuse link: (a) a 50 A 660 V ac fuse link and (b) a silver fuse link element.*

The typical fuse consists of an high conductivity element that is surrounded by a filler and enclosed by the fuse body. The element is welded or soldered to the fuse contacts (blades or ferrules). The fuse element is one or more parallel conductors of pure silver rolled into thin bands, 0.04 to 0.25 mm thick. Each silver band has a number of traverse rows of punched holes (or notches) as shown in figure 12.3. The area between the holes determines the pre-arcing I^2t integral of the fuse and, along with thermal aspects, is related to the fuse current rating. The number of rows of holes determines the fuse voltage rating. When fusing occurs the current is shared between the holes (the necks - weak spots), while the arcing voltage is supported between the series of rows of holes. The arcing characteristics are enhanced by packing the silver element in a filler, such as sand or glassed sand (quartz). The sand and silver element are contained in a ceramic body and the element is welded or soldered to the fuse contacts (blades or ferrules). These end connector plates are copper flashed and tinned. The element is a calibrated conductor where its configuration, mass, and the materials employed are selected to achieve the desired electrical and thermal characteristics. During normal operation, the I^2R heat generated by the element is absorbed by the sand and transferred through the fuse body to the surrounding air. When an overload current occurs, the element generates heat at a faster rate than the heat can be transferred to the sand. If the overload persists, the element reaches its melting point, melts

and then open circuits with an arc. The glass filler aids fuse performance by absorbing (quenching) arc energy and reduces 'burn-back' when the fuse clears an overload or short circuit.
Increasing the applied current will heat the element faster and cause the fuse to open sooner. Thus fuses have an inverse time current characteristic, that is, the greater the over-current the less time required for the fuse to open the circuit. This characteristic is desirable because it parallels the characteristics of conductors, motors, transformers, and other electrical apparatus.

The initial basic selection criteria for determining the necessary fuse's rated amperage does not involve the influence from overload and cyclic loading or the fault capabilities of the load. The actual RMS steady-state load current passing through the fuse should be less than or equal to the calculated maximum permissible load current called I_b.

$$I_b = I_n \times A_t \times K_e \times B_v \times C_f \times K_a \times K_b \qquad (12.1)$$

where:

- I_b = Maximum permissible continuous RMS load current
- I_n = Nominal rated current of a given fuse
- A_t = Ambient temperature correction factor (Figure 12.4a)
- K_e = Thermal connection factor (Figure 12.4b)
- B_v = Cooling air correction factor (Figure 12.4c)
- C_f = Frequency correction factor (Figure 12.4d)
- K_b = Fuse load constant. (Normally 1.0 for porcelain body fuses and 0.8 for fibre body fuses.)
- K_a = High altitude correction factor, given by equation (12.2)

$$K_a = \frac{I}{I_n} = \left(1 - \left(\frac{h - 2000}{100} \times \frac{0.5}{100}\right)\right) \qquad (12.2)$$

where:

- I = Current rating at high altitude
- I_n = The fuse's rated current
- h = Altitude, m

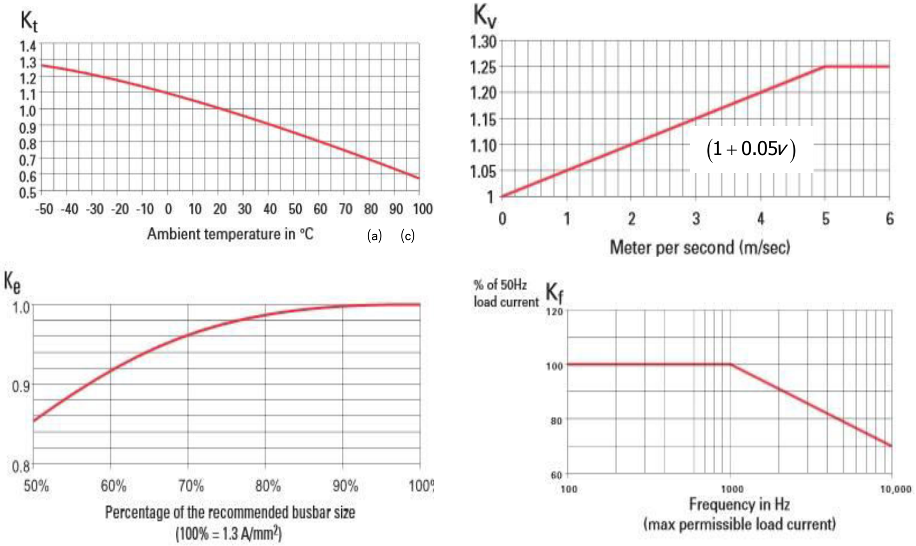

Figure 12.4. *Correction parameters of a fuse during steady state operation rating: (a) ambient temperature K_t; (b) thermal correction K_e; (c) air cooling correction B_v; and (d) frequency correction C_f.*

Practically, a fuse's maximum permissible steady-state load current Ib can be checked by making simple voltage measurements under actual operating conditions. This should be done after the fuse is installed in its operating location and loaded at the calculated I_b value:

$$\frac{E2}{E1} \times \left(0.92 + 0.004 \times T_a\right) \leq N \qquad (12.3)$$

where:

- E_1 = Voltage drop across fuse after 5 seconds
- E_2 = Voltage drop across fuse after 2 hours
- T_a = Air temperature at start of test in C°
- N= Constant (if available, typically 1.5 or 1.6)

Example 12.1 ***AC circuit fuse link design, in steady state***

A 200A porcelain square body fuse is applied at an ambient temperature of 40°C, and wired with cables having a 120mm^2 cross section.
Forced air-cooling is applied at a rate of 4 m/s, while the load current frequency is 3kHz.
What is the maximum allowed steady-state RMS current I_b?
To accurately estimate the correct permissible load of the square body fuse it is necessary to evaluate each correction factor to the application.

Solution

From the current determining formula in equation (12.1), and the correction factors shown in Figure 12.4 parts a to d:

$$I_b = I_n \times A_t \times K_e \times B_v \times C_f \times K_a \times K_b$$

where:

- I_n = 200 A
- A_t = 0.9 for 40C° ambient (Figure 12.4a)
- K_e = 0.98 at 78% (Figure 12.4b)
- Current density= 200 A/120 mm^2 = 1.54 A/mm^2
- % density = 1.3/1.54= 78%
- B_v = 1.2 for 4m/s forced air cooling (Figure 12.4c)
- C_f = 0.85 for a frequency of 3000 Hz (Figure 12.4d)
- K_a = 1, at sea level, below 2000 meters, equation (12.2)
- K_b = 1.0 porcelain body fuse load constant

which results in:

I_b= 200 x 0.9 x 0.98 x 1.2 x 0.85 x 1 x 1 = 180A RMS

The 200A fuse should only be subjected to a maximum 180A RMS under the described steady-state conditions. (see ***12.2.1vi***)

♣

Other factor which deteriorate a fuses rating are over loads and their duration, and rate of occurrence.

The action of a typical fuse link is shown in figure 12.4. Owing to the rms *prospective fault current* I_a the fuse melts at point A, time t_m. Depending on the fuse design and the circuit, the current may continue to rise further to point B, termed the *peak let-through current* I_p. Beyond this point the impedance of the arcing fuse forces the fault current down to zero at the point C. Thus *fuse-clearing* or *total interrupting time* t_c consists of a *melting time* t_m and an *arcing time* t_a.

A series *L-R* circuit can be used to model the prospective fault. The current characteristic is given by

$$i_{sc}(\omega t) = \sqrt{2}\, I_a \left\{ \sin(\omega t - \psi - \phi) - \sin(\psi - \phi)\, e^{-\omega t / \tan\phi} \right\} \qquad (12.4)$$

(12.5)

where ψ is the angle of the short circuit, after the zero voltage cross-over. $\tan\phi = \omega L / R$. The maximum peak fault current therefore occurs when the short appears at zero voltage cross-over, $\psi = 0$.

Differentiation of equation (12.4) gives the current *di/dt*, and the maximum initial *di/dt* is

$$\left.\hat{di}/dt\right|_{t=o} = \sqrt{2}\, I_a \times \sin\psi / \sin\phi \qquad (12.6)$$

This equation shows that the maximum initial *di/dt* occurs for a short circuit occurring at the peak of the ac supply, $\psi = ½\pi$, and is independent of the circuit *R-L*, that is independent of ϕ.

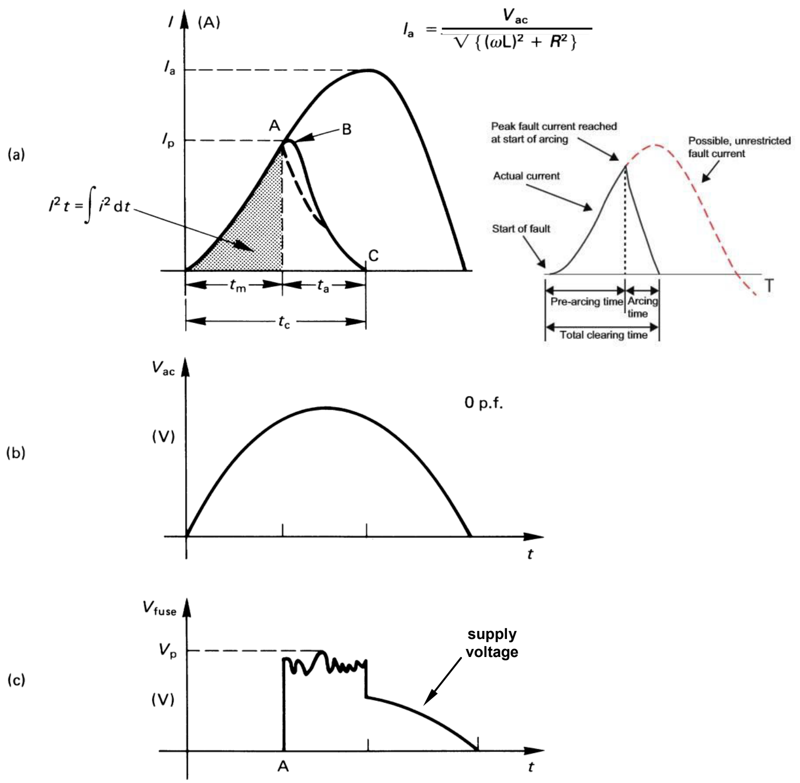

Figure 12.4. *Parameters of a fuse link operating: (a) current waveforms; (b) supply voltage; and (c) fuse arcing voltage.*

The load fault energy, for a fuse link resistance R, is

$$W_{tot} = \int_0^{t_c} i_{sc}^2 R\,dt \qquad \text{(J)}$$

If the load current, shown in figure 12.3a, during fuse action is assumed to be triangular, then the clearing integral of the fuse is

$$W_c = \tfrac{1}{3} I_p^2 t_c R \qquad \text{(J)} \qquad (12.7)$$

If the resistance R is assumed constant (because of its low resistivity temperature co-efficient), the value of I^2t ($\tfrac{1}{3} I_p^2 t_c$) is proportional to the energy fed to the protected circuit. The I^2t term is called the *total let-through energy* or the *virtual clearing integral* of the fuse. The energy which melts the fuse is proportional to $\tfrac{1}{3} I_p^2 t_m$ and is termed the *pre-arcing* or *melting* I^2t.

12.2.1i - Pre-arcing I^2t

Before a fuse melts, the fuse is affected only by the current flowing. The pre-arcing or melting I^2t characteristics of fuse links are therefore only a function of prospective fault current and are independent of voltage. For melting times longer than 5 to 10 ms, the time-current characteristics are usually used for design. Typical time-current characteristics for four different current rated fuses are shown in figure 12.5. For times less than a millisecond, the melting I^2t reduces to a minimum and the pre-arcing I^2t characteristics shown in figure 12.6 are most useful.

The peak let-through current I_p, is a function of prospective fault current I_a for a given supply voltage. Typical current cut-off characteristics are shown in figure 12.7.

12.2.1ii - Total I^2t let-through

For fuse operating times of less than about 10 milliseconds the arcing I^2t can be considerably larger than the pre-arcing I^2t and it varies considerably with system voltage, fault level, power factor, and the point on the wave when the fault is initiated. The higher the voltage the more onerous is the duty of the fuse link because of the increase in energy absorbed by the fuse link during the arcing process. Under short-circuit conditions this leads to an increase in I^2t let-through with voltage. The I^2t let-through will decrease with increased supply frequency whereas the cut-off current will increase.

The peak arc voltage after melting is usually specified for a given fuse link type and is a function of supply voltage, as indicated by the typical arcing voltage characteristics in figure 12.8. The faster the fault is cleared, the higher the arc voltage V_p. Typical total I^2t let-through values for total operating times of less than 10ms, at a given voltage, are shown in figure 12.9. Derating factors for temperature, frequency, and power factor are shown in figure 12.10.

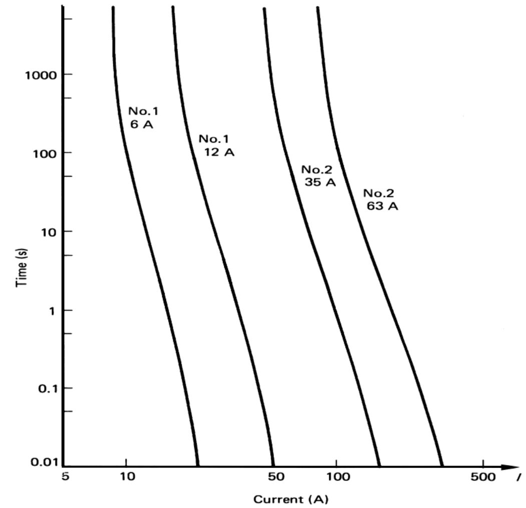

Figure 12.5. *Fuse-link time-current characteristics for 4 fuses and symmetrical sinusoidal 50Hz currents.*

12.2.1iii - Fuse link and semiconductor I^2t co-ordination

Difficulties arise in matching fuses with semiconductors because each has very different thermal and electrical properties.

Semiconductor manufacturers publish (mainly for diodes and thyristors) I^2t withstand values for their devices for times less than 10ms. To ensure fuse link protection the total I^2t let-through by the fuse link under appropriate circuit conditions should be less than the I^2t withstand ability of the semiconductor.

Fuse link manufacturers usually give the data shown in figures 12.5 to 12.10. In ac applications the parameters on which the semiconductor withstand capability is normally compared to the fuse link are

- Peak let-through current versus clearing time or clearing I^2t
- Applied voltage
- Power factor

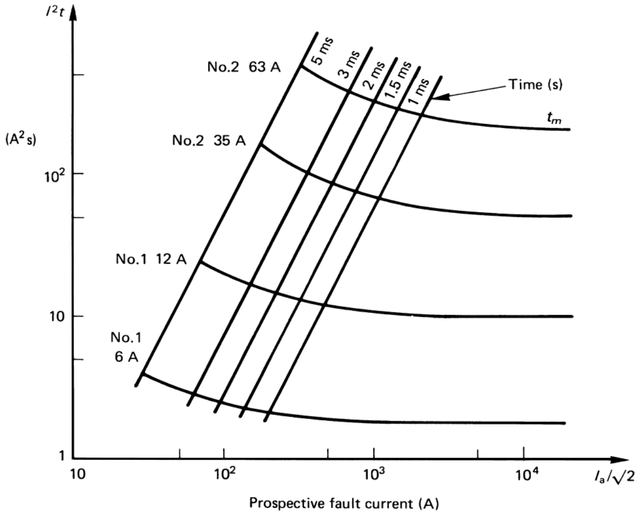

Figure 12.6. *Pre-arcing I^2t characteristics of four fuse links.*

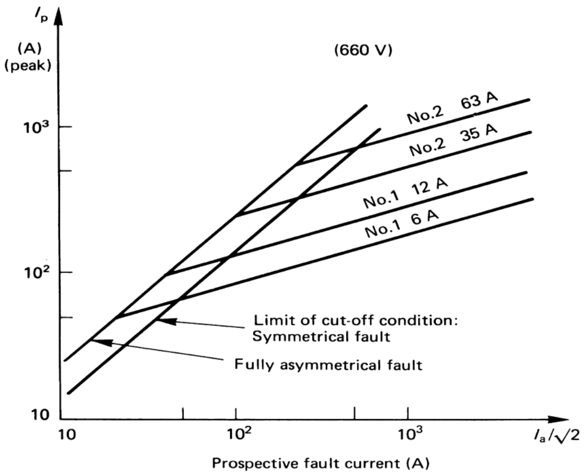

Figure 12.7. *Fuse-link cut-off characteristics at 660 V rms.*

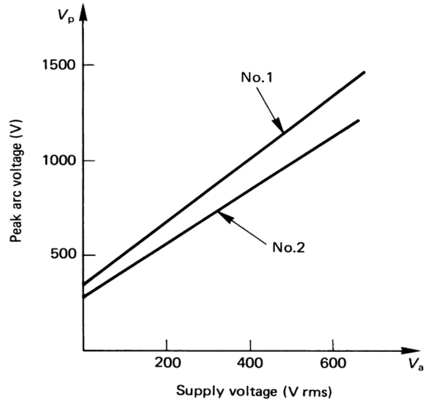

Figure 12.8. *Typical peak arc voltage for two different fuse-link types.*

The voltage rating indicates that the fuse can be relied upon to safely interrupt its rated short circuit current in a circuit where the voltage is equal to, or less than, its rated voltage. The standard voltage ratings used by fuse manufacturers for small dimension and midget fuses are 32, 63, 125, 250 and 600.
In electronic equipment with relatively low output power supplies, with circuit impedance limiting short circuit currents to values of less than ten times the current rating of the fuse, it is common practice to specify fuses with 125 or 250 volt ratings for secondary circuit protection of 500 volts or higher.
As mentioned previously, fuses are sensitive to changes in current, not voltage, maintaining their 'status quo' at any voltage up to the maximum rating of the fuse. It is not until the fuse element melts and arcing occurs that the circuit voltage and available power become an issue.
To summarize, a fuse may be used at any voltage that is less than its voltage rating without detriment to its fusing characteristics.

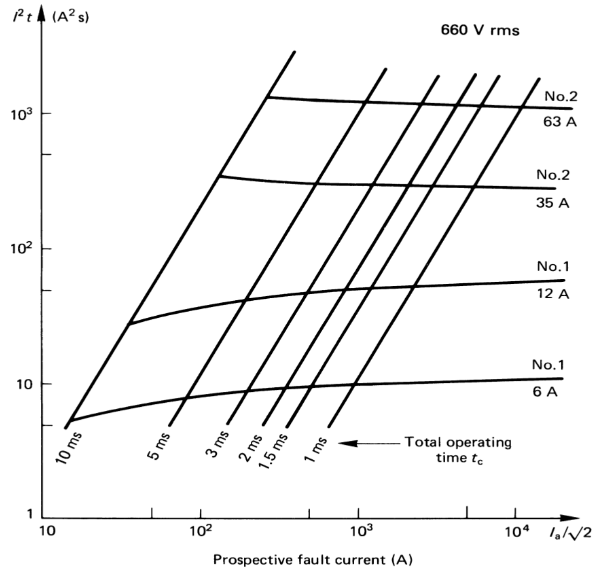

Figure 12.9. *Total let-through current*
for total fuse-link operating times of less than 10ms and at 660V rms.

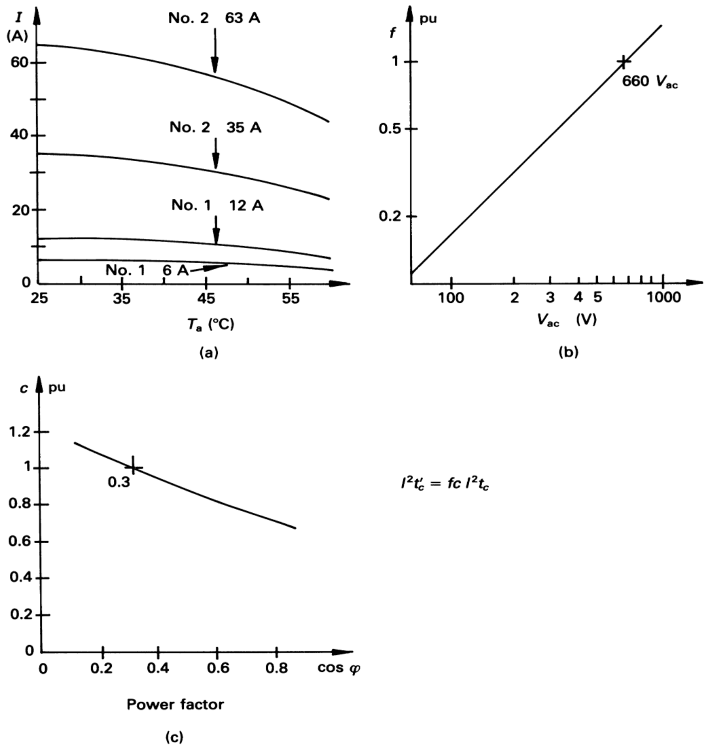

Figure 12.10. *Fuse derating with: (a) ambient temperature; (b) ac supply voltage; and (c) power factor.*

12.2.1iv – Fuse link derating and losses

For 25ºC ambient temperatures, it is recommended that fuses be operated at no more than 75% of the nominal current rating established using the controlled test conditions. Fuses are essentially temperature-sensitive devices whose ratings have been established in a 25ºC ambient. Even small variations from the controlled test conditions can greatly affect the predicted life of a fuse when it is loaded to its nominal value, usually expressed as 100% of rating.

To compensate for variable operating factors, for trouble-free, long-life fuse protection of equipment, the fuse should not be used at more than 75% of the nominal rating, whilst ensuring overload and short circuit protection must be adequately provided for. The fuse temperature generated by the current passing through the fuse increases with increased ambient temperature. Increased ambient temperature decreases the nominal current rating of a fuse. Most traditional fuse designs use lower melting temperature materials and are, therefore, more sensitive to ambient temperature changes.

The resistance of a fuse is usually an insignificant part of the total circuit resistance. Since the resistance of fractional amperage fuses can be several ohms, this fact should be considered when using them in low-voltage circuits. Most fuses are manufactured from materials which have positive temperature coefficients, and, therefore, it is common to refer to cold resistance and hot resistance (voltage drop at rated current), with actual operation being somewhere in between. Cold resistance is the resistance obtained using a measuring current of no more than 10% of the fuse's nominal rated current. Hot resistance is the resistance calculated from the stabilized voltage drop across the fuse, with current equal to the nominal rated current flowing through it.
The maximum permissible continuous fuse current I_b is dependant on the ambient temperature T_{amb} and the air flow velocity (see figure12.4c), according to

$$I_b \le I_n \times \left(1 - 0.005 \times \left(T_{amb} - 20^\circ\text{C}\right)\right) \times \left(1 + 0.05v\right) \times K_b \qquad (12.8)$$

where I_n is the fuse rated current and the air velocity, v, is limited to 5m/s (no beneficial effect results above this velocity). The fuse load constant K_b is assumed worst case, that is 100% conduction, K_b = 1.

In the absence of manufacturer's curves as in figure 12.10a, being a resistive element, fuse losses are related to the square of the current, that is

$$P_{n\%} = \left(\frac{n\% \text{ of } I_{rated}}{100\% \text{ of } I_{rated}}\right)^2 \times P_{100\%} = \left(\frac{I_{load}}{I_n}\right)^2 \times P_{100\%} \qquad (12.9)$$

where $P_{100\%}$ is the fuse losses at rated current I_n in a 20°C ambient.

Example 12.2: ***AC circuit fuse link design***

A fast acting fuse is connected in series with a thyristor in a 415 V ac, 50 Hz ac application. The average current in the thyristor is 30 A at a maximum ambient temperature of 45°C. The ratings of the thyristor are

$I_{T(AV)}$ = 45 A @ T_c = 85°C
I_{TRMS} = 80 A
I^2t = 5 k A^{2}s for 10 ms @ 125°C
I^2t = 20 k A$^2\sqrt{s}$
I_{TSM} = 1000 A for 10 ms @ 125°C and V_{RRM}= 0

The fault circuit inductance is 1.32 mH and the resistance is negligible. Using figures 12.5 to 12.10, select a suitable fuse.

Solution

From figure 12.10a, the 35 A rms No. 2 fuse is rated at 30 A rms in a 45°C ambient.
From figure 12.8 the peak arc voltage for a type No. 2 fuse will be less than 1200 V, hence the thyristor voltage rating must be greater than 1200 V and possibly 1200V+√2×415V ac, depending on the point-on-wave of the fault and the particular circuit configuration.
The short circuit or prospective rms symmetrical fault current is

$$I_{sc} = \frac{I_a}{\sqrt{2}} = \frac{V_s}{X_L} = \frac{415\text{V}}{2\pi \times 50\text{Hz} \times 1.32\text{mH}} = 100\text{A}$$

Figure 12.6 gives a fuse peak let through current of 500 A, which is less than the thyristor peak current rating, I_{TRMS}, of 1 kA.
Figure 12.9 gives the fuse total I^2t of 300 A^{2}s and the total clearing time of t_c =3.5 ms. Since the fuse clears in less than 10ms (½ ac cycle), the thyristor re-applied V_{RRM} will be zero and an I_{TSM} = 1000 A rating is applicable. The total I^2t is corrected for voltage (415V ac) and power factor (0 pu) with f = 0.6 and c = 1.2 from figures 12.10b and c.

$$I^2t' = f \times c \times I^2t = 0.6 \times 1.2 \times 300 \text{ A}^2\text{s} = 216 \text{ A}^2\text{s}$$

which is significantly less than the thyristor I^2t rating of 5 kA^{2}s.
Since t_c is less than 10 ms, the $I^2\sqrt{t}$ rating of the thyristor is used.

$$I^2t'' = (I^2\sqrt{t})\,\sqrt{t_c}$$
$$= 20 \text{ kA}^2\sqrt{s} \times \sqrt{3.5 \text{ ms}} = 1.18 \text{ kA}^2\text{s}$$

which is significantly greater than the I^2t (216 A^{2}s) of the fuse.

Since the fuse peak let through current (500 A) is less than the thyristor peak surge current rating (1000 A), and the fuse I^2t rating (216 A^{2}s) is significantly less than that for the thyristor (1180 A^{2}s), the proposed 35 A fast acting fuse should afford adequate protection for the thyristor.
Generally, if the rms current rating of the fuse is less than the average current rating of the thyristor or diode, the fuse will provide adequate protection under fault conditions.

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12.2.1v – Pulse derating

Here the general term 'pulses' is used to describe the broad category of wave shapes referred to as 'surge currents', 'start-up currents', 'inrush currents', and 'transients'. Electrical pulse conditions vary considerably from one application to another and different fuse constructions may not react the same to a given pulse condition. Electrical pulses produce thermal cycling and possible mechanical fatigue that could affect the fuse life. Initial or start-up pulses are normal for some applications and require the characteristic of a '*slow blow*' fuse, incorporating a thermal delay design to enable it to survive normal start-up pulses and still provide protection against prolonged overloads. The start-up pulse should be defined and then compared to the time-current curve and I^2t rating for the fuse.
Nominal melting I^2t is a measure of the energy required to melt the fusing element and is expressed as 'Ampere squared seconds' (A^{2}s). This nominal melting I^2t, and the energy it represents (within a time

duration of 8ms [0.008 s] or less and 1ms [0.001 s] or less for thin film fuses), is a value that is constant for each different fusing element. Because every fuse type and rating, has a different fusing element, it is necessary to determine the I^2t for each. This I^2t value is a parameter of the fuse itself and is controlled by the element material and the configuration of the fuse element. In addition to selecting fuses on the basis of normal operating currents, derating, and ambient temperature, it is also necessary to apply the I^2t design approach. This nominal melting I^2t is constant for each fuse element design and is also independent of temperature and voltage. The nominal melting I^2t method of fuse selection is applied to those applications in which the fuse must sustain large current pulses of a short duration. These high-energy currents are common in many applications and are critical to the design analysis.

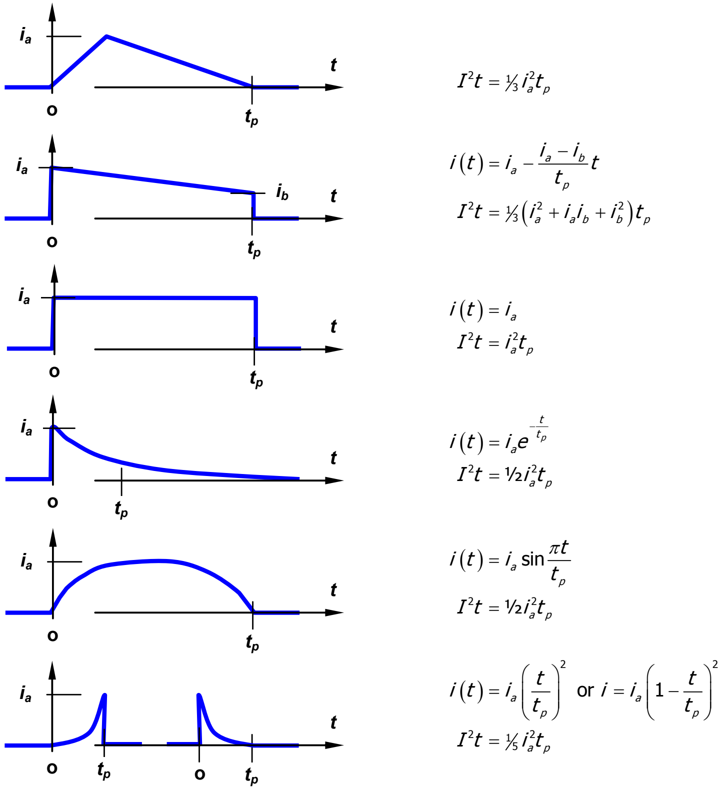

Figure 12.11. *Fuse I^2t formula for various current waveforms.*

The following example illustrates the application of I^2t for a fusing undergoing repetitive surges.

Example 12.3: ***AC circuit fuse link design for I^2t surges***

Based on figures 12.6 and 12.11, select a 230V, very fast-acting fuse that is capable of withstanding 100,000 pulses of current having a triangular pulse waveform of 20A magnitude and of 3ms duration. The normal operating current is 4.5A at an ambient temperature of 25ºC.

Solution

At 25ºC, no fuse thermal derating is necessary.
The first waveform and the associated effective pulse I^2t formula in figure 12.11 are applicable, where i_p=20A and the effective duration is 3ms.

The applicable value for peak pulse current i_p and time t into the corresponding formula for the first wave-shape in figure 12.11 gives:

$$I^2t = \frac{1}{3} i_p^2 t$$
$$= \frac{1}{3} \times 20^2 \times 3\text{ms} = 0.40\text{A}^2\text{s}$$

This value is referred to as the *pulse I^2t*.

The required nominal melting I^2t value for 100,000 occurrences of the calculated pulse I^2t from figure 12.12, involves a derating figure of 22%. The calculated pulse I^2t is converted to the necessary nominal melting I^2t values as follows:

$$\text{Nominal Melt } I^2t = \frac{\text{Pulse } I^2t}{22\%}$$
$$= \frac{0.4}{0.22} = 1.82 \text{ A}^2\text{s}$$

Examine the I^2t rating data for a 230V, very fast-acting fuse. From figure 12.6, the 6A design is rated at 2A^{2}s, which is the minimum fuse rating that will accommodate the 1.82A^{2}s value calculated. This 6A fuse will also accommodate the specified 4.5A normal operating current, when a 25% derating factor is applied to the 6A nominal rating.

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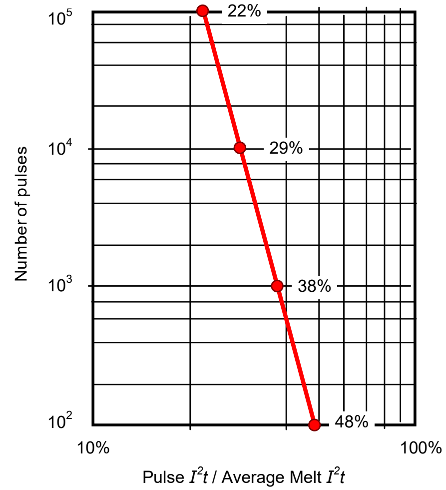


Figure 12.12. *Fuse pulse number derating curves, assuming adequate cooling time between pulses.*

12.2.1vi - Other fuse link derating factors (see figure 12.4)

Ambient temperature correction coefficient, A_t (see figure 12.4a)
Fuse current ratings are usually established at a reference ambient air temperature T_{ref} of 25°C or 30°C. Typical ambient operating temperatures are greater, T_{op}, so the fuse must be derated. The temperature rise depends on the internal power dissipation, which is a function of the current squared. The derating coefficient, for a maximum allowable fuse temperature of T_{max} (typically 130°C to 150°C), is

$$A_t = \sqrt{\frac{T_{max} - T_{op}}{T_{max} - T_{ref}}}$$

Forced cooling correction coefficient, B_v
Forced air cooling, up to a limit about v=5m/s, increases the fuse continuous rating by up to 25%, according to (see figure 12.4c):

$$B_v = 1 + 0.05 \times v \le 1.25$$

Terminal conductor size coefficient K_b
Connected cables and busbars conduct heat away from the fuse, thereby affecting the fuse temperature. A factor 0.8 to 1 can account for busbar conduction and the effects of nearby heat sources. Liquid cooling of the terminals can result in a correction factor of greater than one.

High frequency derating coefficient C_f (see figure 12.4d)
The fuse link element is a metal strip, in which at fundamental frequencies f above 1kHz, its resistance is increased by skin effects. The I^2R losses are increased, where the current includes harmonics, which should not exceed 15% more than the fundamental. The derating is applicable from 100Hz up to 20kHz is shown in the following table. The function $C_f = 1 - 0.075 \times \log_{10} f$ may be applicable for certain fuses.

F Hz	C_f
$0 < f \le 100$	1.0
$100 < f \le 500$	0.95
$500 < f \le 1{,}500$	0.9
$1{,}500 < f \le 5{,}000$	0.8
$5{,}000 < f \le 10{,}000$	0.7
$10{,}000 < f \le 20{,}000$	0.6

Current-variation coefficient A_i
Large rms current variations cause thermal fatigue of the small notch zones on the fuse link used for semiconductor fuses. The thermal derating is classified as either continuous or cyclic.
On/off operation a few time per day with minimal overloads is considered continuous operation, and has an associated 20% derating, A_i = 0.8. Equipment turned on and off once per day, or less often, is fuse derated by 10%, A_i = 0.9.
Cyclic loading is when the fuse heats and cools to steady-state at a cycle rate of less than a few tens of minutes, $A_i \le 0.6$.

The fuse current rating for a nominal current I_n is derated to a maximum rms continuous current (12.1) of

$$I_n' = I_n \times A_t \times B_v \times K_b \times C_f \times A_i$$

Example 12.4: ***AC circuit fuse link derating***

A 1000A fuse has following operational data:
maximum operating temperature T_{max} = 150°C
reference temperature T_{ref} = 30°C
modest busbars giving C_1 = 0.85

The operational environment is:
ambient temperature T_{op} = 50°C
fundamental frequency f = 1kHz
forced air cooling velocity v = 2m/s
operation: cyclic every hour, A_i = 0.6

What is the maximum allowable continuous current I_b for the fuse?
.
Solution

From the frequency derating table C_f = 0.9 at 1kHz.

$$A_t = \sqrt{\frac{T_{max} - T_{op}}{T_{max} - T_{ref}}} = \sqrt{\frac{150°C - 50°C}{150°C - 30°C}} = 0.91$$

$$B_v = 1 + 0.05 \times v = 1 + 0.05 \times 2m/s = 1.1$$

$$\begin{aligned} C_f &= 1 - 0.075 \times \log_{10} f \\ &= 1 - 0.075 \times \log_{10} 1000Hz = 0.775 \end{aligned}$$

The fuse adjusted rating is

$$\begin{aligned} I_b &= I_n \times A_t \times B_v \times K_b \times C_f \times A_i \\ &= 1000A \times 0.91 \times 1.1 \times 0.85 \times 0.9 \times 0.6 = 460A \end{aligned}$$

The adjusted rating of 460A is significantly lower than the 1000A applicable to rated fuse conditions.
♣

12.2.1vii – Fuse link dc operation
Fuse link protection in dc circuits presents greater difficulty than for ac circuits. No natural ac period current zeros exist and faults can result in continuous arcing. In steady state DC systems, inductors become conductors with no resistance and capacitors become open circuits; therefore, the only circuit component to consider is resistance. For operating times greater than 1 second, the heating effect of an AC current is the same as DC current and the characteristics merge. . Figure 12.13 shows a typical AC peak let-through and time-current curve (red) along with DC peak let-through and time current curve at time-constants of 25ms (green) and 80ms (blue). A higher DC time constant shifts the curves up for the peak let-through, and the time-current curves to the right.

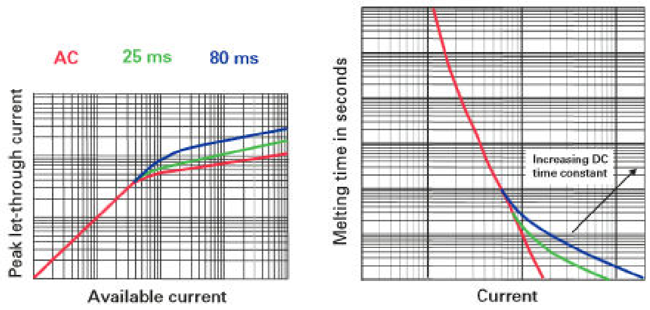


Figure 12.13 *AC and DC operating characteristics merge for operating times greater than 1 second.*

Fuses should not be used to clear low overcurrents in DC circuits. For a high speed fuse to effectively operate, the fault current must be high enough to quickly melt the fuse element. The fault current's rate of rise (time constant) has to be fast enough to allow the fuse to clear the DC arc generated during fault clearing. Table 12.2 show typical L/R time constants with various power electronics applications. DC fusing of applications involving dc machine shunt field windings is problematic. DC fault conditions are difficult to properly fuse, and misapplication may cause a fuse stress failure.

Table 12.2: Typical *L/R* time constants applicable to various power equipment

application	*L / R* time constant (ms)
Plastic/paper capacitor bank	< 0.1
Electrolytic capacitor bank	< 1
Supercapacitor bank	< 1 (τ=RC=800ms)
Battery	< 10
Three phase generated dc bus	< 25
DC motor armature	20 -60
DC traction system	40 - 100
Rotating machine dc field (dc machine shunt winding)	1000

In the transient case, the breaking (or interrupting) capacity of a fuse link in a dc application depends on

- the maximum applied dc voltage, $\hat{E}$
- the feed *L /R* time constant, τ
- the maximum prospective short circuit current of the circuit, I_a
- pre-arcing I^2t of the selected fuse

Some high-speed semiconductor ac fuses can be used in dc applications (but should be avoided), after suitable derated. There is no safe conversion of a fuse AC voltage rating to a DC voltage rating.
The rate of current rise, specified by the circuit time constant L/R influences the energy input rate that melts the fuse's element. This influences both the fuse's melting time-current characteristic and the peak let-through current. The longer the fault current L/R time constant, the lower the allowable operating voltage, since the fuse takes longer to melt due to the slower energy delivery rate. Conversely, the higher the prospective short-circuit current I_a, the faster the fuse operates hence it can operate at a higher dc voltage level.

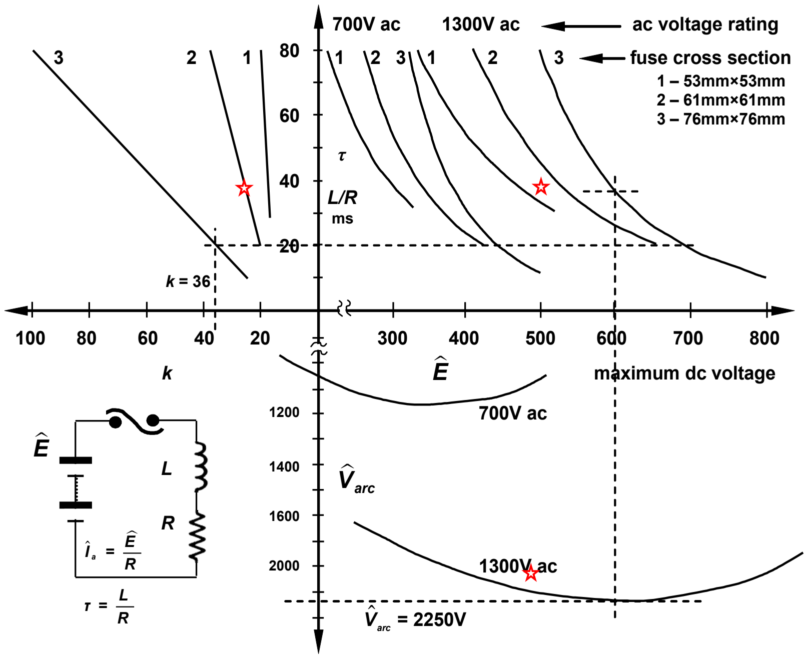


Figure 12.14. *Design curves for an ac fused used in dc applications.*

Typically, the fuse dc rating is 70% of its ac voltage rating for time constants between 10ms to 20ms, and the dc capability rating decreases as the circuit time constant increases. No voltage derating is necessary for time constants less than 2½ms.
Published fuse characteristics and performance data generally concentrate on ac at 50 Hz or 60 Hz. values. The design monograph in figure 12.14 can be used to select a suitable ac high-speed fuse for dc application. The design requires the fault time constant $\tau = {}^{L}\!/_{R}$, which will specify the maximum allowable dc voltage $\hat{E}$, whence the maximum dc arcing voltage $\hat{V}_{arc}$. The fault time constant also specifies the pre-arcing (from cold) I^2t derating factor k, used to specify the minimum prospective fault current $\check{I}_a$ to ensure enough energy for the fuse to melt, thence clear.

$$\check{I}_a = k\sqrt{I^2t} \qquad (12.10)$$

This minimum current must be less than the prospective peak dc fault current given by

$$I_a = \frac{E}{R} \qquad (12.11)$$

That is, $\check{I}_a < I_a$ is a fuse link requirement.

The instantaneous fault current is $i(t) = I_a(1-e^{-t/\tau})$, while the instantaneous rms current is

$$i_{rms}(t) = I_a\sqrt{1 + \frac{2e^{-n}}{n} - \frac{e^{-2n}}{2n} - \frac{1.5}{n}} \quad \text{where} \quad n = {}^{t}\!/_{\tau}\text{, the number of time constants} \qquad (12.12)$$

Example 12.5: *DC application of an AC circuit fuse link*

A dc circuit conforms to: applied voltage E=500Vdc and the short circuit L and R are 0.64mH and 16mΩ. Is the interrupt rating of a fuse with the following specification adequate:

- 1300 Vac
- 1100 A
- Size 3/110
- 580,000 A²s (I^2t pre-arcing integral)

What is the maximum expected arcing voltage?

Solution

The prospective short-circuit current I_p is

$$I_p = \frac{E}{R} = \frac{500\text{V}}{16\text{m}\Omega} = 31.3\text{kA}$$

and time constant (L/R) is

$$\tau = \frac{L}{R} = \frac{0.64\text{mH}}{16\text{m}\Omega} = 40\text{ms}$$

From the first quadrant of figure 12.14, for an applied voltage of 500Vdc and a 40ms time constant, Curve 2 must be used (1200Vac square body fuse with a 61mmx61mm cross-section). A 700Vac fuse is completely inadequate in this application. From the same figure, 4th quadrant, for L/R = 40 ms on Curve 2, k = 25.

For a fuse pre arcing I^2t of 570,000 A²s, a minimum prospective current of 31.3kA must exceed

$$\check{I}_a = k\sqrt{I^2t} = 25 \times \sqrt{570{,}000\text{ A}^2\text{s}} = 20\text{kA}$$

From the 2nd quadrant, the maximum expected arcing voltage is approaching 2.2kV.

♣

Example 12.6: *DC circuit fuse link design*

A traction 600V dc supply has an equivalent source impedance of 20mΩ and 0.4mH, and a nominal dc load current of 600A.

i. Validate the suitability of the following ac fuse in being able to safely clear a dc fault current.
ii. Estimate the fuse losses at 20°C ambient.
iii. What is the maximum nominal current allowable in an air still 80°C ambient?
iv. Estimate the fuse losses in the 80°C ambient.

FUSE: High speed 900A, 1300V ac, with a pre-arcing I^2t of 505,00A²s at room temperature, in a case size #3 of cross section 75mm×76mm, allowing 125W of losses at 20°C.
Figure 12.14 is applicable to this fuse link element.

Solution

The maximum applied voltage is $\hat{E}$ = 600V dc
The short circuit fault time constant is $\tau = {}^{L}\!/_{R} = {}^{0.4\text{mH}}\!/_{20\text{m}\Omega} = 20\text{ms}$

i. From figure 12.14, a size #3 fuse will offer better voltage and current overheads than a type #2 fuse. The data yields k = 36, an arcing voltage maximum of 1920V dc, and would allow fault time constants of up to 36ms or peak dc supply voltages of up to 700V dc.

The prospective short circuit fault current from equation (12.11) is

$$I_a = {}^{E}\!/_{R} = {}^{600\text{V}}\!/_{20\text{m}\Omega} = 30\text{kA}.$$

From equation (12.10), the minimum allowable fault current to ensure enough energy to melt and clear the fuse is

$$\check{I}_a = k \times \sqrt{I^2t}$$
$$= 36 \times \sqrt{505{,}00} = 25.6\text{kA}$$

Since $\check{I}_a < I_a$, that is, 25.6kA < 30kA, the fuse will reliably and predictably melt, thence clear.

ii. The 125W fuse loss at rated current of 900A is reduced if the nominal load current is 600A. From equation (12.9):

$$P_{n\%} = \left(\frac{I_{load}}{I_n}\right)^2 \times P_{100\%}$$
$$= \left(\frac{600\text{A}}{900\text{A}}\right)^2 \times 125\text{W} = 55½\text{W}$$

iii. At ambient temperatures above 20°C, the fuse nominal current rating is decreased according to equation (12.8):

$$\hat{I} \le I_n \times \left(1 - 0.005 \times (T_{amb} - 20°\text{C})\right) \times (1 + 0.05 \times v) \times K_b$$
$$\le 900\text{A} \times \left(1 - 0.005 \times (80°\text{C} - 20°\text{C})\right) \times (1 + 0.05 \times 0) \times 1$$
$$\le 900\text{A} \times (1 - 0.005 \times 60°\text{C}) = 630\text{A}$$

Thus the fuse would be satisfactory at 80°C with the nominal load current of 600A dc.

iv. The fuse losses at 600A in an 80°C ambient would be approximately

$$P = \left(\frac{I_{load}@80°\text{C}}{\hat{I}@80°\text{C}}\right)^2 \times P_{100\%}$$
$$= \left(\frac{600\text{A}}{630\text{A}}\right)^2 \times 125\text{W} = 113\text{W}$$

♣

12.2.1viii – Alternatives to dc fuse operation

It may be possible in some applications to use an ac fuse in a dc circuit, before the rectification stage. Generally low voltage fuses are more effective than high voltage fuses. In high voltage transformer applications satisfactory protection may be afforded by transferring the fuse to the low voltage side. The fuse I^2t rating is transferred as with impedance transferring, that is, in the turns ratio squared.

$$I^2t_{fuse}^{primary} = \left(\frac{V_s}{V_p}\right)^2 \times I^2t_{semiconductor}^{secondary} \qquad (12.13)$$

Alternatively an mcb (miniature circuit breaker) may offer better protection in cases when the ac fault is more of an overload such that the current magnitude is limited. On overload, the mcb takes a longer time to clear than a fuse, thus the mcb is less prone to nuisance tripping. Aspects of both dc and ac relays and contactors, including dc and ac mcb's, are presented in Chapter 33.

Fuse protection is mainly applicable to more robust devices such as thyristors and diodes. Transistors (MOSFETs more readily than IGBTs, even when avalanche rated) usually fail as a result of over-current before any fuse link can clear the fault.

12.2.2 Protection with resettable fuses

Resettable fuses are basically thermistors. Thermistors are thermally sensitive resistors and have, according to type, a negative (NTC), or positive (PTC) resistance/temperature coefficient.

PTC (positive temperature coefficient) thermistors are ceramic or polymeric crystalline protection components whose electrical resistance rapidly increases as a certain temperature is exceeded.

Over-current circuit protection can be accomplished with the use of either a traditional fuse-link or PTC device. PTC devices are typically used in a wide variety of electronics applications where over-current events are common and automatic resettability is desired. This ability of a PTC device to reset itself after experiencing a fault current makes it ideal within circuits that are not readily accessible or where a constant uptime is required.

There are two types of PTC thermistors based on different underlying materials: polymer and ceramic, as summarised in Table 12.3. Generally the device cross-sectional area determines the surge current capability, and the device thickness determines the surge voltage capability.

Thermal Properties

The operation of all PTC devices is based on an overall energy balance described by equation (12.14), which assumes a uniform temperature distribution within the device:

$$H\frac{\Delta T}{\Delta t} = I^2R - U \times (T - T_A) \qquad \text{(W)} \qquad (12.14)$$

where

I = current flowing through the device, A
R = resistance of the device, Ω
Δt = change in time, s
H = heat capacity, $H = m \times c_p$, J/ K
m = mass of the device, kg
c_p = heat capacity of the PTC thermistor device, J/kg K
ΔT = change in device temperature, K
T = device temperature, K
T_A = ambient temperature, K
U = effective heat-transfer coefficient, heat dissipation factor, $U=h\times A$, W/K

In equation (12.14), the current flowing through the device generates heat at a rate equal to I^2R. All or some of this heat is lost to the environment, at a rate described by the term $U\times(T - T_A)$. Any heat not lost to the environment raises the device temperature at a rate described by the term $mc_p\times(\Delta T/\Delta t)$.

If the heat generated by the device and the heat lost to its environment balance, then in this steady-state equilibrium condition, $\Delta T/\Delta t$ tends to zero and equation (12.14) reduces to:

$$I^2R = U \times (T - T_A) \qquad \text{(W)} \qquad (12.15)$$

Under normal operating conditions, this thermal steady-state is at a relatively low temperature and in the low resistance region, as indicated by operating *Point 1* in Figure 12.15.

The thermal characteristics of PTC devices are similar to those of the NTC devices, and can be described by the following terms:

- heat capacity, *H,* in J/K
- heat dissipation constant, *D,* in W/K
- thermal time constant, *τ,* in seconds

Heat capacity

The product of the specific heat and mass of the thermistor, heat capacity is the amount of heat required to produce a 1K change in the body temperature of the thermistor.

$$H = m \times c_p$$

Ceramic PTC thermistors have a heat capacity of about 3J/cm^3/K.

Heat dissipation constant

The heat dissipation factor is the amount of heat which is lost, over a unit of time, based on a 1K temperature difference between the heating element and ambient temperature.

It is the ratio of the change in the power applied to the thermistor to the resulting change in body temperature due to self-heating. The factors that affect the dissipation constant including: lead-wire materials, method of mounting, ambient temperature, conduction or convection paths between the device and its surroundings, and the structure, shape, and material of the PTC device itself.

$$P = IxV = U(T - T_A) = U\Delta T \qquad \text{(W)}$$

T: temperature of heating element, K
U: heat dissipation factor, W/K

Thermal time constant

The time required for the thermistor temperature to change 63.2% of the difference between the self-heated temperature and the ambient after the power is disconnected. The thermal time constant is also influenced by the same environmental factors as those that affect the dissipation constant.

The thermal time constant *τ* is the time to reach 0.632 times the temperature difference between T and T_A.

$$\tau = \frac{H}{U} \qquad \text{(s)} \qquad (12.16)$$

U: heat dissipation factor, W/K
H: heat capacity, J/K

12.2.2i Polymeric PTC devices

Polymeric PTC materials

Polymeric positive temperature coefficient circuit protectors are made from a conductive plastic formed into thin sheets, with electrodes attached to either side of the compressed stacked sheets. The conductive plastic matrix is manufactured from a nonconductive crystalline polymer and dispersed highly-conductive carbon black particles, typically high density polyethylene mixed with graphite. The plate electrodes ensure even distribution of power loss through the device, and provide a surface for leads to be attached or for surface mounting. The phenomenon that allows conductive plastic materials to be used for resettable over-current protection devices is that they exhibit a large non-linear positive temperature coefficient effect when heated. A PTC is a thermal characteristic that many materials exhibit whereby resistance increases with temperature. What makes a PTC conductive plastic material unique is the magnitude of its resistance increase. At a specific transition temperature, the increase in resistance is so large that it is characterised on a logarithmic scale.

Resettable over-current polymeric PTC protector physics

The conductive carbon black filler material in the PTC device is dispersed in a polymer that has a crystalline structure. The crystalline structure densely packs the carbon particles into its crystalline boundary so they are close enough together (beyond a level called the percolation threshold) to allow current to flow through the polymer insulator via the created carbon 'chains', due to a tunnelling effect. When the conductive plastic is at room temperature, there are numerous carbon chains forming parallel conductive paths through the mostly crystalline material.

Under electrical fault conditions, excessive current flows through the PTC device. Internal I^2R Joule heating causes the conductive plastic material's temperature to rise. As this self-heating continues, the material's temperature continues to rise until it exceeds its phase transformation temperature. As the material passes through this phase transformation temperature, the densely packed crystalline polymer matrix changes to an amorphous structure, disrupting the network of conductive carbon paths. This phase change is accompanied by a small volumetric expansion. As the conductive particles move apart from each other, most no longer conduct current and the resistance of the device increases sharply.

The material will stay 'hot', remaining in this high resistance state as long as the power is applied. This latched state provides continuous fold-back protection, until the electrical fault is cleared and the power is reduced. Reversing the phase transformation, by cooling, allows the carbon chains to re-form as the polymer re-crystallizes. The resistance quickly reduces toward its original low value.

Principle of operation

Both polymeric positive temperature coefficient thermistor protectors and traditional fuse-link devices react to internal I^2R Joule heat generated by an excessive current flow in a circuit. Whereas a fuse-link melts open, interrupting the current flow, a PTC device restricts current flow as its bulk rises in temperature, changing from a low to a high resistance state. In both cases, this transitional condition is termed *tripping*. The characteristic curve in figure 12.15 shows the typical response of a PTC device to temperature.
If the current through the device is increased while the ambient temperature is maintained constant, the heat generated within the device increases and the temperature of the device also increases. Whilst the increase in current is modest, if the generated heat can be lost to the environment, the device will stabilize according to equation (12.15) at a higher temperature, such as *Point 2* in Figure 12.15.
Alternatively, instead of the current being increased, the ambient temperature is raised, the device will stabilize according to equation (12.15) at a higher temperature, possibly again at *Point 2*. *Point 2* could also be attained by a combination of both a current increase and an ambient temperature increase.
Further increase in either current, ambient temperature, or both will cause the device to reach a temperature where the resistance begins to rapidly increases, such as at *Point 3* in Figure 12.15. Any further increase in current or ambient temperature will cause the device to generate heat at a rate greater than the rate at which heat can be transferred to the environment, thus causing the device to heat up rapidly. A large increase in resistance occurs for a small change in temperature. In Figure 12.15, this region of large change in resistance for a small change in temperature occurs between points 3 and 4, and this operating region is termed the *tripped state*. This large increase in resistance causes a corresponding decrease in the current flowing in the down-line series circuit.
The resultant current reduction reduces the likelihood of circuit damage. Since the temperature change between operating points 3 and 4 is small, the term $(T - T_A)$ in equation (12.15) can be replaced by the constant $(T_{op} - T_A)$, where T_{op} is the operating temperature of the device. Then equation (12.14) becomes:

$$I^2R = \frac{V^2}{R} = U \times (T_{op} - T_A) \qquad \text{(W)} \qquad (12.17)$$

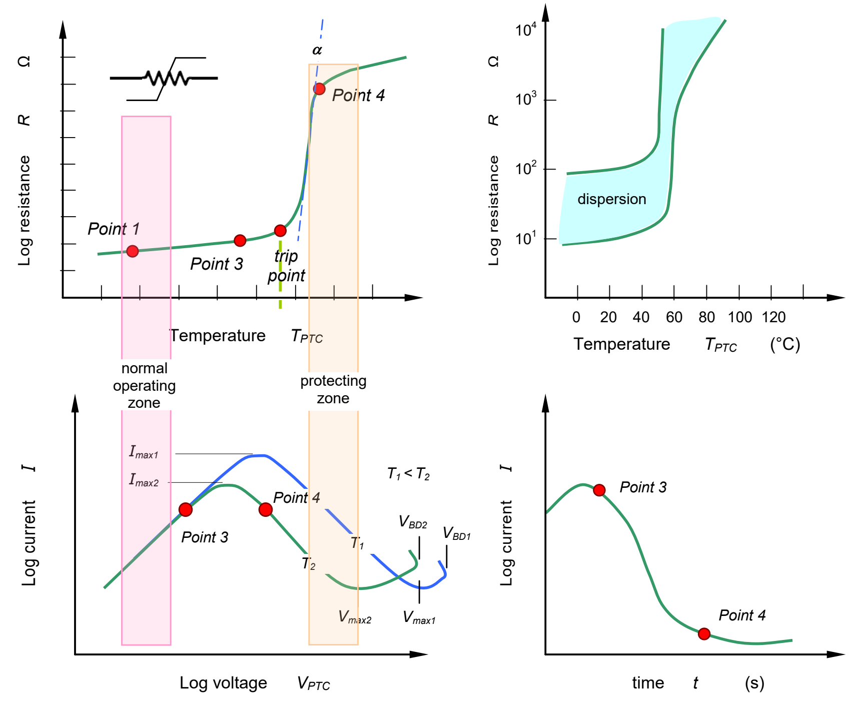


Figure 12.15. *Polymeric PTC thermistor operating R-V-I-t curves and typical tripping dispersion.*

Since both U and $(T_{op} - T_A)$ are now constants, equation (12.17) reduces to a constant, I^2R = constant; that is, the device now operates in a constant power state. Expressing this constant power as V^2/R emphasizes that, in the tripped state, the device resistance is proportional to the square of the applied voltage. This relation holds until the device resistance reaches the upper knee of the curve, *Point 4* in Figure 12.15.
For a device that has tripped, as long as the applied voltage is high enough for the resulting V^2/R power to maintain the $U\times(T_{op} - T_A)$ loss, the device remains in the tripped state, that is, the device will remain latched in its protective high-resistance state. When the voltage is decreased to the point where the $U\times(T_{op} - T_A)$ loss can no longer be supplied, the device begins to reset to a lower resistance state, by traversing back along the R-T characteristic towards *Point 1*.

Electrical Properties

The electrical characteristics describing PTC devices (ceramic and polymeric) include the following:

- current-time characteristic
- resistance-temperature characteristic
- voltage-current characteristic
- power and minimum resistance
- temperature coefficient of resistance
- transition temperature
- voltage and frequency dependence
- voltage rating

Hold and trip current

Figure 12.16 illustrates the hold-current and trip-current behaviour of PTC devices as a function of device bulk temperature.

Region A represents the combinations of current and temperature at which the PTC device will trip (go into the high-resistance state) and protect the circuit. *Region B* describes the combinations of current and temperature at which the PTC device will allow for normal operation of the circuit, a low resistance state. In *Region C*, it is possible for the device to either trip or remain in the low-resistance state, depending on the individual device resistance. The boundaries between these regions are defined as the hold and trip currents.

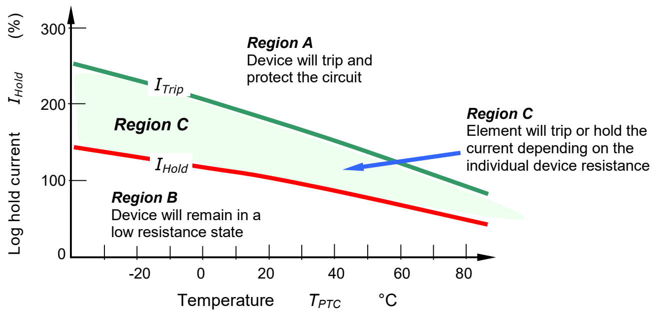


Figure 12.16. *Polymeric PTC device hold and trip currents as a function of device temperature.*

Hold current, I_{Hold}, at a given temperature, is the highest steady-state current that a device will hold for an indefinite time without transitional tripping from the low resistance to the high resistance state.

Trip current, I_{Trip}, is the minimum current at which the device will switch from the low resistance to the high resistance state.

The trip current is typically greater than the normal operating current. Unlike time-to-trip, the hold current of a device is a steady-state condition that can be fairly accurately defined by the heat transfer environment. Under steady-state conditions, equation (12.17) is valid and the I^2R heat generated equals the heat lost to the environment. Therefore, if U increases, the hold current increases, with the approximate dependency:

$$I_H \propto \sqrt{U}$$

Since PTC devices are thermally activated, any change in the surrounding temperature will affect device performance. As the surrounding temperature increases, less energy is required to trip the device, thus the hold current decreases. Consequently the I_{Trip} and I_{Hold} curves both have negative slopes in Figure 12.16. Thermal derating curves and I_{Hold} versus temperature tables enable in-circuit design over a wide range of temperatures, as illustrated in example 12.5.

The heat transfer for PTC devices is affected by several factors, for example:

- An increase in the ambient temperature surrounding the device results in a reduction in heat transfer. This can be caused by a general increase in the ambient temperature, or the device being in proximity to a heat-generating source such as a power switching device, resistor or transformer. The hold current, power dissipation, and time-to trip of the device are all reduced.
- By changing the width/area of pcb copper pads or increasing the device lead lengths, which are in thermal contact with the device. A surface mount device on an increased copper pad area, results in an increase in the heat transfer. This results in a higher hold current and power dissipation, and a slower time-to trip.
- If the airflow around the device is increased, heat transfer is increased.

Time-to-trip

The time-to-trip of a PTC device is the time it takes for the voltage drop across the device to rise to greater than 80 percent of the voltage of the power source, or when the resistance of the device increases substantially relative to the load resistance. A trip event is caused when the rate of heat lost to the environment is less than the rate of heat generated, causing the device temperature to increase. The rate of temperature rise and the total energy required to make the device trip, depend on the fault current and the heat transfer environment.

For low-fault currents, for example two-to-three times the hold current, devices trip slowly since a substantial amount of the I^2R generated heat is lost to the environment, therefore only slowly increases the device temperature. This type of trip event can be considered as a non-adiabatic trip event. Under these conditions, the heat transfer to the environment plays a significant role in determining the time-to-trip of the device. The greater the heat transfer, the longer the time-to-trip.

At high-fault currents, for example ten times the hold current, the time-to-trip is reduced because most of the I^2R energy generated is retained in the device, thereby rapidly increasing its temperature. A trip event of this kind can be regarded as an adiabatic trip event. Under these conditions, the heat transfer to the environment is less significant in determining the time-to-trip of the device.

As tripping is a dynamic event, it is difficult to precisely predicted the change in the time-to-trip since a change in the heat transfer coefficient is often accompanied by a change in the thermal mass around the device. If for example the device uses a metal heatsink, not only will the heat transfer increase, but the device will also need to heat some fraction of the metal (due to the intimate thermal contact) before the device will trip. Therefore, not only is the thermal conductivity of the metal important, but the heat capacity of the metal is also a factor in determining the time-to-trip.

The switching time or time-to-trip t_s can be approximated, in an adiabatic condition, by:

$$t_s = \frac{c_p Vol}{P}\left(T_{ref} - T_A\right) \qquad (12.18)$$

T_{ref} reference temperature of PTC thermistor
Vol PTC thermistor volume
P switch-on power of the PTC thermistor

This equation shows that the switching time is influenced by the size of the PTC thermistor, its reference temperature, and the power supplied. Switching times are lengthened by increasing the volume or the reference temperature; while a high power consumption by the PTC thermistor results in short switching times.

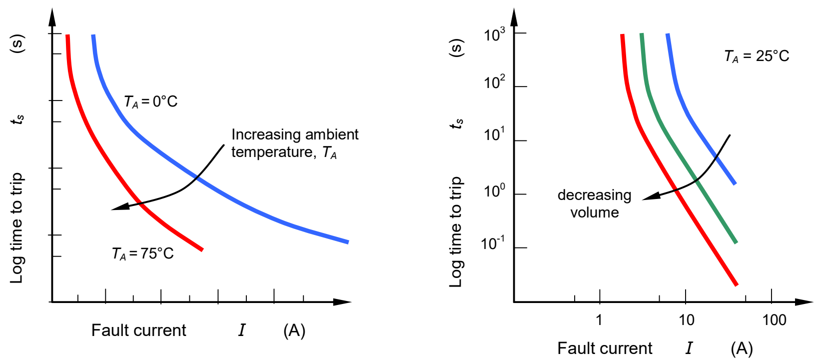


Figure 12.17. *Polymeric PTC curves for a PTC rated at 72V, 40A, with a 1.1A to 3.75A hold current.*

Figure 12.17 shows a typical pair of operating curves for a PTC device in still air at 0°C and 75°C. The curves are separate because the heat required to trip the device comes both from electrical I^2R heating and from the device environment. At 75°C the heat input from the environment is substantially greater than at 0°C, so the additional I^2R needed to trip the device is correspondingly less, resulting in a lower trip current at a given trip time, or a faster trip at a given trip current.

Device reset time

In Figure 12.18, after a trip event (when the current fault condition has been alleviated), the resistance recovery to a quasi-stable low value is rapid, with most of the recovery typically occurring within a few minutes. Figure 12.18 shows the resistance recovery curve and associated power dissipation for a family of leaded PTC fuse devices.

As with other electrical properties, the resistance recovery time depends upon both device design and the thermal environment. Since resistance recovery is related to device cooling, the greater the heat transfer, the quicker the recovery.

Typical recovery resistance after a trip event: trip jump, R_{1MAX}

PTC devices exhibit resistance hysteresis after tripping, either through an electrical trip event or through a thermal event such as reflow soldering.

Figure 12.18 shows typical polymeric PTC device behaviour after tripping and when cooling. It can be seen that even after a number of hours, the device resistance is still greater than the initial pre-trip resistance. Over an extended period, device resistance will continue to fall and will eventually approach the initial resistance. Therefore, when PTC devices are being used, this ‘trip jump’ or ‘reflow jump’ is taken into consideration when determining the hold current. This increase in resistance is defined as R_{1MAX} and the jump is measured one hour after the thermal fault event. The long-term cold resistance of polymeric PTC thermistors increases with successive trip events.

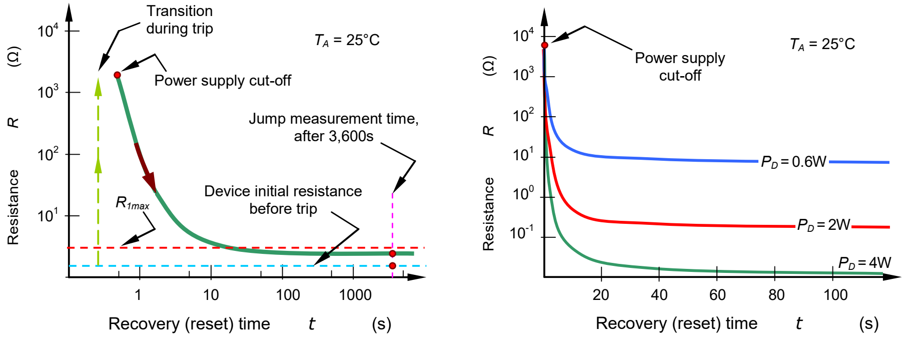


Figure 12.18. *Polymeric PTC typical resistance recovery after a trip event.*

12.2.2ii Ceramic PTC devices

Unlike PTC thermistors made of plastic materials, that is, polymeric materials, ceramic PTC thermistors always return to their initial resistance value, even after frequent heating/cooling cycles.

The thermal properties and many of the electrical properties are characterised the same for both PTC material types.

Ceramic PTC thermistors
Mixtures of barium carbonate, titanium oxide and other materials (become doped polycrystalline ceramic, containing $BaTiO_3$ - 69% plus titanates of Pb - 15%, Sr - 10%, Ca - 5% and 1% dopants), whose composition produces the desired electrical and thermal characteristics are ground, mixed and compressed into various shapes. These blank parts are then sintered, at temperatures just below 1400°C, and after cooling, they are contacted, provided with connection elements, and finally coated or encased. Multilayer or bulk ceramic types are available.

Generally, ceramic is a good insulating material with a high resistance. Semi-conduction and thus a low resistance are achieved by doping the ceramic with materials of a higher valency than that of the crystal lattice. Some of the barium and titanate ions in the crystal lattice are replaced by these higher valencies to obtain a specified number of free electrons which make the ceramic conductive.

The material structure is composed of many individual crystallites. At the edge of these monocrystallites, the so-called grain boundaries, potential barriers are formed. They prevent free electrons from diffusing into adjacent areas. The result is high resistance at the grain boundaries. However, this effect is neutralized at low temperatures. High dielectric constants and sudden polarization at the grain boundaries prevent potential barriers formation at low temperatures enabling a flow of free electrons.

Above the ferroelectric Curie temperature, dielectric constant and polarization decline so far that there is a rapid increase of the potential barrier heights and it becomes difficult for electrons to pass the potential barrier whence the resistivity of the corresponding material rises dramatically. In a specific temperature range above the Curie temperature T_c, the resistance of the PTC thermistor rises exponentially. Beyond the range of the positive temperature coefficient, the number of free charge carriers is increased by thermal activation. The resistance then decreases and exhibits a negative temperature characteristic (NTC) typical of semiconductors, as shown in figure 12.19.

Figure 12.19c shows that over the majority of the PTC thermistor operating temperature range, it exhibits a slight negative temperature coefficient, similar to most semiconductors. However, as the temperature approaches the switch temperature, T_s, or Curie temperature, the resistance of the element begins to rise rapidly. This steep increase in resistance continues as the temperature rises but eventually levels off and the temperature coefficient becomes negative again at higher temperatures.

Switch temperature, T_s
The switch temperature of a ceramic PTC is the temperature at which the resistance of the PTC thermistor begins to increase rapidly. The switch temperature is usually defined as the temperature where the resistance of the element is twice the minimum resistance value R_{min}, $T_s = T(2 \times R_{min})$.

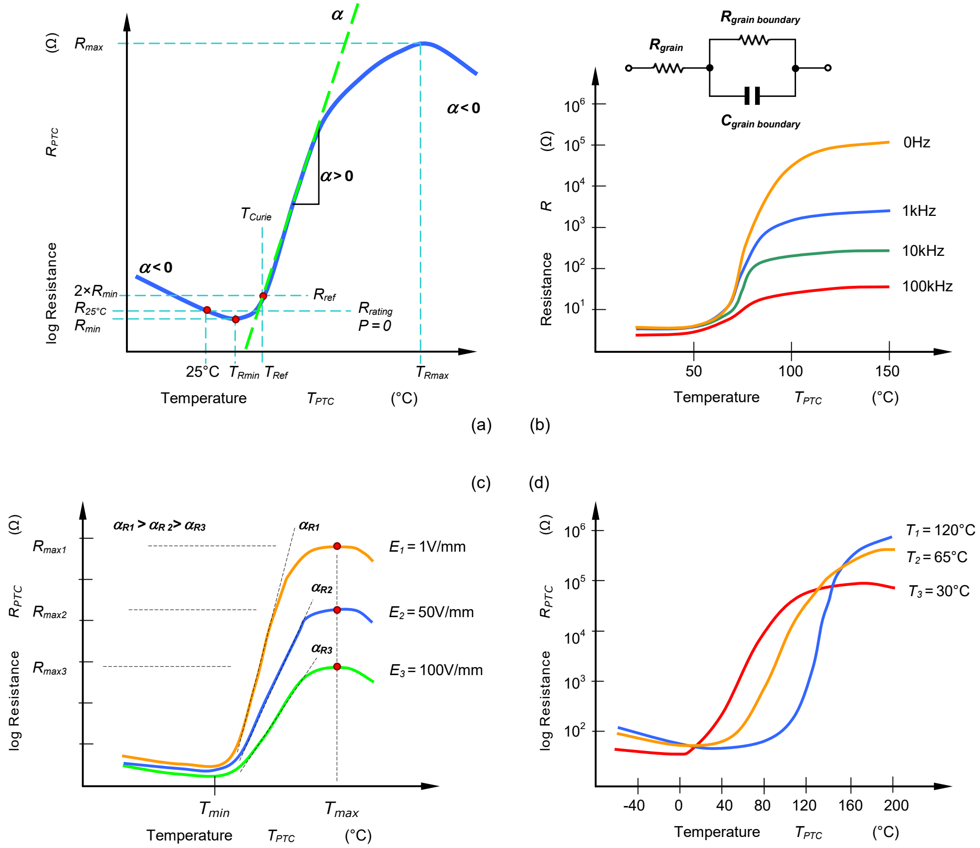


Figure 12.19. *PTC ceramic thermistor: (a) R-T characteristics; (b) influence of frequency on R-T characteristics and ac equivalent circuit; (c) influence of electric field strength E (varistor effect) on R-T characteristics; and (d) reference temperature effect on ceramic R-T characteristics.*

Transitional temperature coefficient, α
The temperature coefficient of resistance α is defined as the relative change in resistance referred to the change in temperature and is calculated for each point on the resistance versus temperature curve by:

$$\alpha = \frac{1}{R}\frac{dR}{dT} = \frac{d\,\ell n\,R}{dT} = \ell n 10 \times \frac{d\,\ell g R}{dT} = 2.3 \times \frac{d\,\ell g R}{dT}$$

In the range of the steep rise in resistance above *Point 3* in figure 12.15, R_{ref}, α is approximately constant. The following relation then applies:

$$R_2 \le R_{PTC} \le R_1 \to \alpha = \frac{\ell n R_2 - \ell n R_1}{T_2 - T_1} = \frac{\ell n \dfrac{R_2}{R_1}}{T_2 - T_1} = \frac{\ell n \dfrac{R_2}{R_1}}{\Delta T}$$

Within this temperature range, the inverse relation gives:

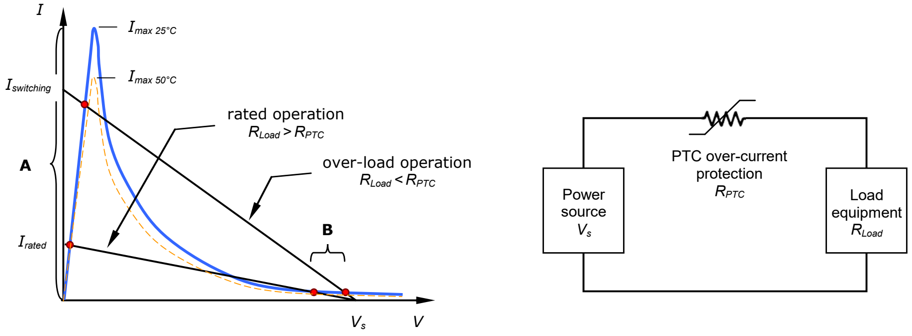
$$R_2 = R_1\, e^{\alpha (T_2 - T_1)} = R_1\, e^{\alpha \Delta T} \qquad (12.19)$$

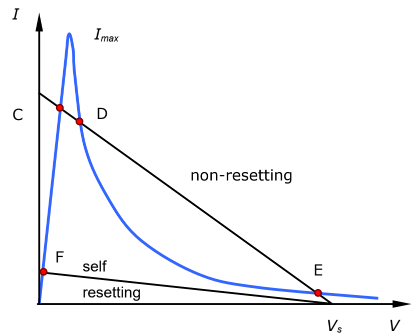
The value of α for the individual types relates only to the temperature range in the steep region of the resistance curve, which is the region of primary interest for most applications.

Voltage dependence of resistance
Higher voltage applied to the ceramic PTC thermistor drop primarily at the grain boundaries with the result that the high field strengths dominating in these regions break-down the potential barriers, thus producing a lower resistance. The higher the potential barriers, the greater the influence of this ‘varistor effect’ on resistance. Below the reference temperature, most of the applied voltage is supported across the grain resistance. Thus the grain boundaries field strength decreases and the varistor effect is weak. These mechanisms result in the increase of alpha and decreases the pre and post trip resistance as the field strength increases as shown in figure 12.19c.

Frequency dependence of resistance
Due to the structure of the PTC thermistor ceramic material, on ac voltages it is not a pure ohmic resistor. It acts as a capacitive resistor because of the grain boundary junction depletion layers. The impedance measured with ac voltages decreases with increasing frequency, as shown in figure 12.19b. The dc tripped resistance is reduced by a factor of over 50 when the element is used at 1kHz, so use of the PTC is generally restricted to DC and line frequency operation.

Protection circuit operation
Figure 12.20 illustrates the two operating states of a PTC fuse. During rated operation of the load the PTC resistance remains low, operating *Point 1* in figure 12.15. Upon overloading or shorting of the load, however, the power consumption in the PTC thermistor increases so much that it heats up, its resistance increases dramatically, and this reduces the current flow to the load to an admissible low level, operating *Point 4* in figure 12.15. Most of the source voltage V_s is then impresses across the PTC thermistor. Although the current is reduced it is sufficient to maintain the PTC in the high-resistance mode, ensuring protection until the cause of the over-current has been removed.





$$I_L = \frac{V_s}{R_{load}} \quad \text{when} \quad T < T_{trip} \quad \text{and} \quad R_{load} > R_{PTC}$$

$$I_L = \frac{V_s}{R_{PTC}} \quad \text{when} \quad T > T_{trip} \quad \text{and} \quad R_{load} < R_{PTC}$$

Figure 12.20. *Polymeric PTC thermistor circuit operating load line, showing the operating states of a PTC thermistor for over-current protection.*

Figure 12.20 illustrates the load-line operating principle of a PTC thermistor designed to operate as a resettable fuse. The region indicated as ‘A’ represents the normal range of current operation. When current exceeds I_{max}, the device self-heating increases its resistance and causes the circuit to operate in the region indicated by B.

The position of the circuit load-line can be designed such that the over-current protection is either automatically reset or requires a manual reset. In the automatic reset mode, the load line intercepts the I-V characteristic at the point F. Stable operation can only occur at this point for normal loads.
In the manual reset mode, the load line intercepts the I-V characteristic at three points in figure 12.20; C, D, and E. Point D is unstable so, in practice, stable operation only occurs at points C and E.

PTC device application
Some of the types of applications that utilize the self-heated characteristics of the PTC thermistor include:

- self-regulating heaters
- over-current protection
- liquid level sensing
- constant current
- time delay
- motor starting
- arc suppression

Generally the device cross-sectional area determines the surge current capability, and the device thickness determines the surge voltage capability. Polymer PTC devices typically have a lower resistance than ceramic PTCs which are stable with respect to voltage and temperature. After experiencing a fault condition, a change in initial resistance occurs with the polymeric PTC.
In balanced systems with a PTC thermistor in each conductor, resistance change may degrade line balance. Including additional series resistance such as a line-feed resistor, LFR, can reduce the effect of the R1 jump. In addition, some PTC thermistors are available in resistance bands to minimize R1 effects. Polymer types are also commonly used singly to protect domestic equipment.
Ceramic PTC devices do not exhibit an R1 jump (because of the reversible ferroelectric Curie temperature mechanism), and their higher resistance avoids the need for installing an LFR. While this reduces component count, the resistance does vary with applied voltage and frequency. Since this change can be substantial (for example, decreasing by a factor of about 3 at 1kV), it is essential that any secondary overvoltage protection be correctly rated to handle the resulting surge current, which can be three times larger than predicted by the nominal resistance of the ceramic PTC. In a typical line application, line balance is critical.

Table 12.3: Characteristics of polymeric and ceramic PTC thermistor fuse devices

PTC Thermistor material	nominal Ohms	Maximum voltage current trip	resistance stability (with voltage and temperature)	resistance change after surge	typical application
Polymer PTC Thermistor	0.01 - 20		Good	10 - 20%	industrial equipment
Ceramic PTC Thermistor	10 - 50	600V, 13A	*R* decreases with temperature and under impulse	small	balanced line

Example 12.7: ***Resettable ceramic fuse design***

A 24V transformer, operating in an ambient temperature range of 20˚C to 60˚C, is to be PTC thermistor protected under the following conditions:
Normal current = 80mA
Fault current = 300mA

Determine if a 50V, 20Ω ceramic device with the following characteristics, is suitable.
The trip current, the minimum must-switch current, is given by

$$I_{Trip} = \sqrt{\frac{\delta \times \left(107 - 0.85 \times T_A^{min}\right)}{0.8 \times R_{25°C}}}$$

The hold current, the maximum no-switch current, is given by

$$I_{Hold} = \sqrt{\frac{\delta \times \left(93 - 0.85 \times T_A^{max}\right)}{1.2 \times R_{25°C}}}$$

where:
δ = 0.008 is the dissipation factor
$R_{25˚C}$ = 20Ω is the nominal resistance at 25˚C

Solution

For this application, the requirements are, a PTC element rated for at least 24V, 50/60Hz, can carry 80mA in a 60˚C ambient, and will switch when conducting less than 300mA at 20˚C.

i. The device maximum rated rms voltage must be greater than the application operational voltage:

$$V_{max} > V_{operational}$$
$$50\text{V ac} > 28\text{V ac}$$

ii. The trip current must be less than the fault current, 300mA:

$$I_{Trip} < I_{fault}$$
$$I_{Trip} = \sqrt{\frac{\delta \times (107 - 0.85 \times T_A^{min})}{0.8 \times R_{25°C}}} = \sqrt{\frac{0.008 \times (107 - 0.85 \times 20°C)}{0.8 \times 20\Omega}}$$
$$= 0.21\text{A} < 0.30\text{A}$$

iii. The hold current (current without switching) must be greater than the normal operating current, 80mA:

$$I_{Hold} > I_{operational}$$
$$I_{Hold} = \sqrt{\frac{\delta \times (93 - 0.85 \times T_A^{max})}{1.2 \times R_{25°C}}} = \sqrt{\frac{0.008 \times (93 - 0.85 \times 60°C)}{1.2 \times 20\Omega}}$$
$$= 0.12\text{A} > 0.08\text{A}$$

The selected PTC fuse is suitable for this transformer protection case.

♣

Traditional Fuses versus PTCs

Fuses and PTC devices are both over-current protection devices, though each offer their own unique operating characteristics and benefits. Understanding the differences between the two technologies makes the selection choice easier, depending on the application. The most obvious difference is that PTCs are automatically resettable whereas traditional fuses need to be replaced after they are tripped, while MCBs must be manually reset. Whereas a fuse and MCB completely stop the flow of current (which may be desired in critical applications) after most similar over-current event, PTCs continue to enable the equipment to function, except in extreme cases.

Because they reset automatically, many circuit designers choose PTCs in instances where over-current events are expected to occur often, and where maintaining low warranty and service costs, constant system uptime, and/ or user transparency are at a premium. They are also often chosen in circuits that are difficult to access in or remote locations, were fuse replacement or MCB reset would be difficult. There are several other operating characteristics to be considered that distinguish PTCs and fuses, and it is also best to test and verify device performance before use within the end application.

- General use PTCs are not rated above 240V while LV fuses are rated up to 600V ac.
- Specifications indicate that similarly rated PTCs have about twice (sometimes more) the resistance of fuses.
- The hold (operating) current rating for PTCs can be up to 14A, while the maximum level for fuses can exceed 30A.
- The useful upper limit for a PTC is generally 85ºC, while the maximum operating temperature for fuses is 125ºC. Ambient temperature effects are in addition to the normal derating. PTCs hold and trip ratings must be derated when applied at conditions other than room ambient. For example, any rise in ambient temperature will decrease the hold current rating as well as the trip current. A reduction in ambient temperature will increase the trip current as well as the hold current.
- Comparing the time-current curves of PTCs to time-current curves of fuses show that the speed of response for a PTC is similar to the time delay of a Slow-Blow fuse.
- When a PTC is in a ‘tripped state’ it protects the circuitry by limiting the current flow to a low leakage level. Leakage current can range from less than a hundred milliamps at rated voltage up to a few hundred milliamps at lower voltages. Fuses (and MCBs) on the other hand completely interrupt the current flow when tripped, and this open circuit results in no leakage current when subjected to an overload current.
- PTCs are rated for a maximum short circuit current at rated voltage, also known as ‘breaking capacity’ or I_{max}. This fault current level is the maximum current that the device can withstand safely, noting that the PTC will not actually interrupt the current flow; it has a leakage current. A typical PTC short circuit rating is 40A; or for the battery strap PTCs, this value can reach 100A. Fuses do in fact interrupt the current flow in response to the overload and the range of interrupting ratings, vary from tens of amperes up to 10,000A at rated voltage.

- A PCT resettable fuse has better defined characteristics in low voltage dc applications, than traditional fuses, in terms of arcing and resultant circuit voltages with inductive circuits.

Table 12.4: Summary of over-current limiters

type		performance						
action	Technology	line at post operation	Speed	accuracy	resistance stability	operating current	series resistance	current rating
Reducing series	Polymer PTC thermistor	reset	fastest	good	poor	low	medium - low	low
	Ceramic PTC thermistor	reset	fast	good	low	low	high	low
interrupting series	Fuse	disconnected	slow	fair	good	medium	low	medium - high
	Line feed resistor	both lines disconnected	poor	poor	good	high	high	low
diverting series/shunt	Heat coil	shorted or open	slow	poor	medium	low	medium	low
diverting series	Thermal switch	shorted	poor	poor	good	high	low	high

12.2.3 Summary of over-current limiting devices

Over-current protection technologies are summarized in Table 12.4, and as follows:

- PTC thermistors provide self-resetting protection.
- Fuses and MCBs provide good overload capability and low resistance.
- Heat coils protect against lower level ‘sneak currents’.
- LFRs provide the most fundamental level of protection, combined with the precision resistance values needed for balanced lines and are often combined with other devices.

An overcurrent protective device must:

- Safely interrupt very high prospective fault currents in extremely short times
- Limit the current allowed to pass through to the protected device
- Limit the thermal energy (I^2t) let-through to the device during fault interruption
- Limit the overvoltage during fault interruption
- Not require maintenance
- Not operate at normal rated current or during normal transient overload conditions
- Operate in a predetermined manner when abnormal conditions occur

The miniature circuit breaker, MCB, a mechanical current controlling device, is considered in 33.19.

12.3 Overvoltage protection

Voltage transients in electrical circuits result from the sudden release of previously stored energy, such as with insulation breakdown arcing, fuses, contactors, freewheeling diode current snap, switches, and transformer energising and de-energising. These induced transients may be repetitive or random impulses. Repetitive voltage spikes are observable but random transients are elusively, unpredictable in time and location. A spike is usually brief but may result in high instantaneous power dissipation. A voltage spike in excess of a semiconductor rating for just a few microseconds usually results in catastrophic device failure. Extensive noise may be injected into low-level control logic causing spurious faults. Generally, high-frequency noise components can be filtered, but low-frequency noise is difficult to attenuate.

Overvoltage devices are placed in parallel with a load or circuitry to be over-voltage protected, to limit the magnitude of the voltage that can appear across the input to a circuit. The overvoltage device appears as a very high-impedance (virtually an open circuit) under normal operating conditions. When an overvoltage event occurs, however, the overvoltage device changes its impedance to divert current through itself, around the protected circuit.

Overvoltage protection devices are designed to protect circuits and additionally, they must:

- Not interfere with normal circuit operation.
- Provide maintenance-free operation.
- Reduce long-term cost of the installation by minimizing maintenance time and system downtime.
- Allow the designer to meet industry standards.

Effective transient overvoltage protection requires that the impulse energy be dissipated in the parallel added transient absorption circuit at a voltage low enough to afford circuit survival.

Clamping and Crowbar Devices

Over-voltage protection devices can be classified as either clamping or fold-back (or crowbar). Zener diodes and metal oxide varistors are clamping devices, since they attempt to clamp the voltage at a defined voltage during a stress event. A crowbar device, such as gas discharge tubes and thyristor surge suppressors attempt to create a short circuit when a trigger voltage is reached, with both cases illustrated in Figure 12.21.

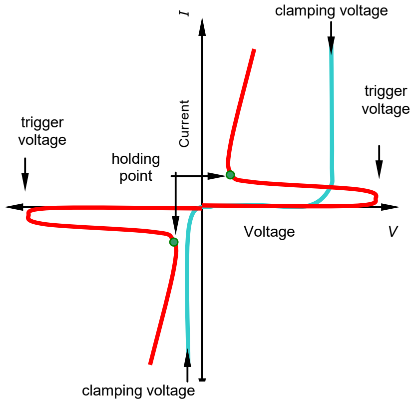


Figure 12.21. *I-V characteristics of a bidirectional crowbar device (black) and a unidirectional clamping device (red).*

Crowbar devices with low on-state voltage can keep voltage levels well below the critical values for sensitive electronic elements and carry considerable current without self-damage due to power dissipation. The lowest current and voltage point that can sustain the on-state of the crowbar device is an important parameter and is often called the holding point, as seen Figure 12.21. If the electrical node being protected can supply the voltage and current levels of the holding point, a crowbar device may not turn off after the electrical stress has been removed. The crowbar device must ensure the protection turns off when the electrical stress is removed and does not turn on during normal operation.

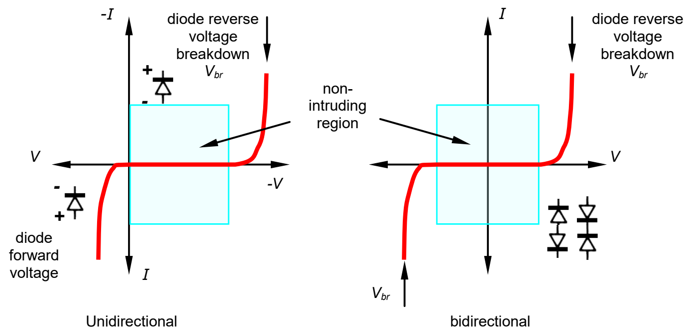


Figure 12.22. *I-V characteristics of: (a) a unidirectional device and (b) a bidirectional device.*

Voltage clamp devices do not have the problem of not turning off after a stress event. Clamping devices protecting dissipate considerable power, which is dissipated internally. Clamping devices need a low dynamic resistance in the on-state to ensure that while carrying large currents the voltage does not exceed the allowed levels for the sensitive circuit elements.

Voltage protection can be classified as either *unidirectional or bidirectional*, as shown in figure 12.22. The clamping device has asymmetrical I-V characteristics, so is classified as unidirectional, while the device with symmetrical I-V characteristics, performs bidirectional clamping. AC circuits generally require suppression which is symmetrical, that is bidirectional.

12.3.1 Transient voltage suppression clamping devices

Two voltage transient suppression techniques can be employed.

- **Transient voltage attenuation**
  Low pass filters, such as an *L-C* filter, can be used to attenuate high frequencies and allow the low-frequency power to flow.
- **Diverter (to limit the residual voltage)**
  Voltage clamps such as crowbars or snubbers are usually slow to respond. The crowbar is considered in section 12.1.3 while the snubber, which is for low-energy applications, is considered in sections 9.2 and 9.3.

The voltage-limiting function may be performed by a number of non-linear impedance devices such as reverse selenium rectifiers, avalanche (commonly called Zener) diodes, and varistors made of various materials such as silicon carbide or zinc oxide.
The relationship between the current in the non-linear device, I, and the voltage across its terminals, V, is typically described by the power law

$$I = kV^{\alpha} \quad \text{(A)} \qquad (12.20)$$

k is an element constant dependent on device geometry and material in the case of the varistor, and the non-linear exponent α is defined as

$$\alpha = \frac{\log I_2 - \log I_1}{\log V_2 - \log V_1} = \frac{\log\ I_2 / I_1}{\log V_2 / V_1}\left(= \frac{1}{\log V_2 / V_1}\right) \qquad (12.21)$$

where I_1 and I_2 are taken a decade apart, $I_2 / I_1 = 10$. The term alpha, α, represents the degree of non-linearity of the conduction. The higher the value of alpha, the better the clamp and therefore alpha may be used as a figure of merit. Linear resistance has an alpha of 1 and a conductance of $k = 1/R$ ($I = \frac{1}{R} V^{+1}$).
The non-linear voltage-dependent static and dynamic resistances are given by

$$R = \frac{V}{I} = \frac{V}{kV^{\alpha}} = \frac{1}{k} \times V^{1-\alpha} \quad (\Omega) \qquad (12.22)$$

$$R_{dyn} = \frac{dv}{di} = \frac{1}{\alpha k V^{\alpha-1}} = \frac{V}{\alpha I} = \frac{R}{\alpha} \quad (\Omega) \qquad (12.23)$$

and the power dissipation is

$$P = VI = V\,kV^{\alpha} = k \times V^{\alpha+1} \quad \text{(W)} \qquad (12.24)$$

The most useful transient suppressors are the Zener diode and the varistor. They are compact devices which offer nanosecond response time and high energy absorption capability.

1 - The Zener diode, usually called a *Transient Voltage Suppressor*, **TVS** in voltage suppression applications, is an effective clamp and comes the closest to being a constant voltage clamp, having an alpha of 35. Since the avalanche junction area is small and not highly uniform, substantial heating occurs in a small volume. The energy dissipation of the Zener diode is limited, although transient absorption Zener devices with peak instantaneous powers of 50 kW are available. These peak power levels are obtained by:

- Using diffusion technology, which leads to low metallisation contact resistance, narrow base width, and minimises the temperature coefficient.
- Achieving void-free soldering and thermal matching of the chip and the large area electrodes of copper or silver. Molybdenum buffer electrodes are used.
- Using bulk silicon compatible glass passivation which is alkali metal contamination free, and is cut without glass cracking.

Voltage ratings are limited to 280V but devices can be series connected for higher voltage application. This high-voltage clamping function is unipolar and back-to-back series connected Zener diodes can provide high-voltage bipolar symmetrical or asymmetrical voltage clamping.

2 - The varistor (variable res**istor -** voltage-dependant resistance inversely related to voltage) is a ceramic, bipolar, non-linear semiconductor utilising silicon carbide for continuous transient suppression or sintered zinc oxide for intermittent dissipation. Approximately 90 per cent by weight of zinc oxide and suitable additives such as oxides of bismuth, cobalt, manganese and other metal oxides, when pressed, can give varistors with alphas better than 25. The micro-structure of the plate capacitor like body consists of a matrix of highly conductive (and high thermal conductivity) zinc oxide grains separated by highly resistive inter-granular grain boundaries of the additive oxides. Micro-varistors are only produced where the sintered zinc oxide grains meet, providing pn junction semiconductor-type characteristics, as shown in figure 12.23a. The grain sizes vary from approximately 100μm in diameter for low-voltage varistors down to 10μm for high voltage components, producing 30 to 250V/mm (typically 2V to 3V per grain boundary junction). The junctions block conduction at low voltage and provide non-linear electrical characteristics at high voltage. Effectively pn junctions are distributed in parallel and series throughout the structure volume, giving more uniformly distributed heat dissipation than the plane structure Zener diode. The diameter (parallel conduction paths over the area) determines current capability, hence maximum power dissipation, while thickness (number series connected micro-varistors) specifies voltage, as indicted by the I-V characteristics in figure 12.23b. A greater number of adjacent boundaries in series and parallel (that is, the volume of the device) leads to higher energy absorption capability. The structure gives high terminal capacitance values (which decreases with voltage rating according to V^{-1}) depending on area, thickness, and material processing. The varistor may therefore be limited in high-frequency applications (>1kHz), due to CV^2f related losses. Functionally the varistor is similar to two identical Zener diodes connected back-to-back, in series.

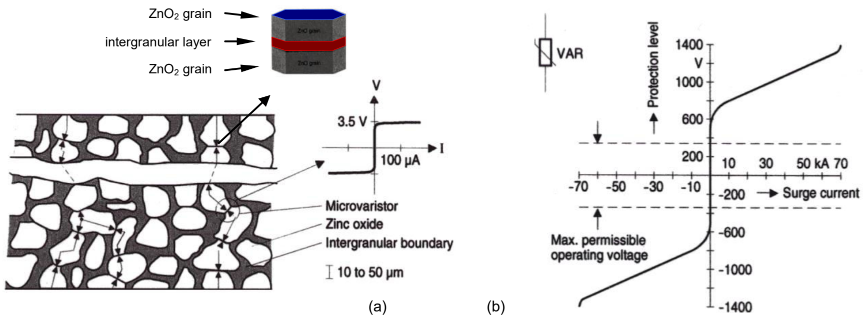


Figure 12.23. *Varistor: (a) conduction mechanisms and (b) I-V linear characteristics.*

Figure 12.24a shows the general equivalent circuit models for the varistor, which consists of the inter-granular boundary resistance R_{IG}, ($\rho \approx 10^{12}$ to 10^{13} Ωcm) the ohmic bulk resistance R_B of the zinc oxide ($\rho \approx$ 1 to 10Ωcm), and the non-linear varistor resistance R_{VAR},(0 to ∞Ω).

Leakage current region, $I < 10^{-4}$

Figure 12.24b show the model when the inter-granular boundary resistance R_{IG} dominates the resistance $R_B << R_{IG}$, giving α = 1, as shown in figure 12.25a. R_{IG} is temperature (negative) dependant, decreasing with temperature, producing increased leakage current, hence higher steady-state standby losses.

Normal operating region, $I > 10^3$

In figure 12.24c, with $R_{VAR} << R_{IG}$ and $R_B << R_{VAR}$, R_{VAR} dominates electrical behaviour, giving α > 30, as shown in figure 12.25a.

High current clamping region, $10^3 > I > 10^{-5}$

In figure 12.24d, the resistance is low as $R_{VAR} << R_{IG}$ and $R_{VAR} < R_B$, giving α = 1, as shown in figure 12.25a, with the ohmic bulk resistance R_B of the zinc oxide dominating.

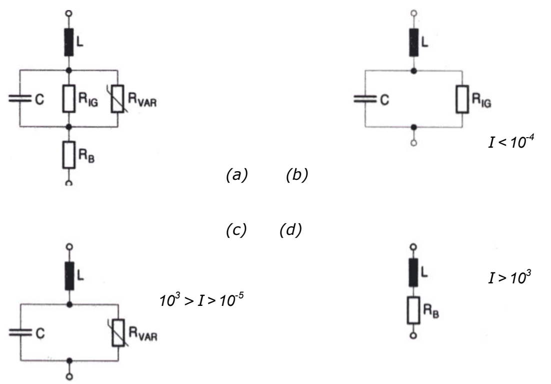


Figure 12.24. *Varistor equivalent circuit models:*
(a) complete model; (b) low current; (c) normal operating region model; and (d)high current model.

The inter-granular capacitance *C*, measured at 1kHz and has a positive temperature coefficient, <0.1%/K, increases with increased thickness (increased voltage rating) and decreases with increase area (increased current/power rating). The capacitance acts as a high pass filter, but restricts the operating frequency limit due to ½CV^2f transferred losses.

The lead inductance (≈1nH/mm) L limits the element transient response (L/R), hence lead length should be minimised.

The varistor voltage rating is the voltage drop across the element when the current is 1mA, at 25°C.

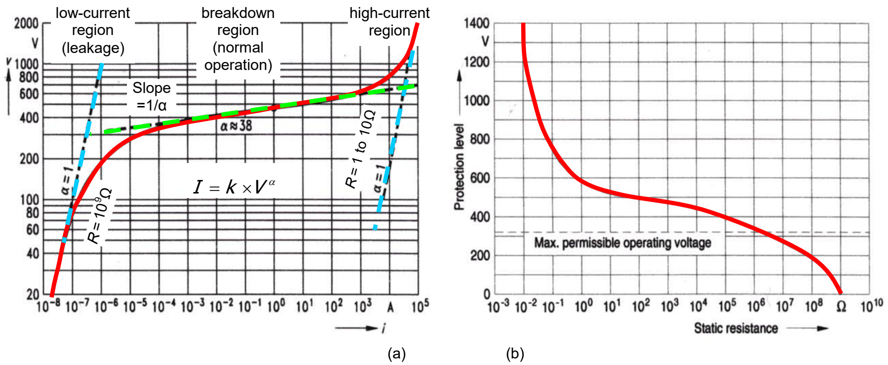


Figure 12.25. *Varistor: (a) I-V linear and (b) static resistance characteristics.*

12.3.1i - Comparison between Zener diodes and varistors (also see Chapter 15.1.3iv)

Figure 12.26a illustrates the I-V characteristics of various voltage clamping devices suitable for 240 V ac application. The resistor with alpha equal to 1 is shown for reference. It is seen that the higher the exponent alpha, the nearer an ideal constant voltage characteristic is attained, and that the Zener diode performs best on these grounds. When considering device energy absorption and peak current and voltage clamping level capabilities, the Zener diode loses significant ground to the varistor.
The higher the alpha, the lower will be the standby power dissipated. Figure 12.26b shows the dependence of standby power dissipation variation on withstand voltage for various transient absorbers. A small increase in Zener diode withstand voltage produces a very large increase in standby power dissipation. Various device compromises are borne out by the comparison in Table 12.5.
The current, power, and energy ratings of varistors typically are rated values up to 85°C, then linearly derated to zero at a case temperature of 125°C. Voltage-limiting diodes are typically linearly derated from rated values at 75°C to zero at 175°C. Reliability depends on the ambient temperature and applied voltage, and lifetime decreases with increased voltage or temperature. In the case of the varistor, an 8 per cent increase in applied voltage halves the mean time between failures, mtbf, for applied voltages less than 0.71 times the nominal voltage. Below 40°C ambient, the mtbf for a varistor is better than 7 x 10^8 hours (0.7 fit).
The voltage temperature coefficient for the varistor is - 0.05 per cent/K while +0.1 per cent/K is typical for the power Zener (at 1mA).

The following design points will specify whether a Zener diode or varistor clamp is applicable and the characteristics of the required device.

- Determine the necessary steady-state voltage rating.
- Establish the transient energy to be absorbed by the clamp.
- Calculate the peak transient current through the clamp.
- Determine power dissipation requirements.
- Determine the clamping voltage to which the transient is to be suppressed.
- Estimate the number of fault cycles during the lifetime.

In order to meet higher power ratings, higher voltage levels or intermediate voltage levels, Zener diodes or varistors can be series-connected. The only requirement is that each series device has the same peak current rating. In the case of the varistor this implies the same disc diameter. Then the I-V characteristics, energy rating, and maximum clamping voltages are all determined by summing the respective characteristics and ratings of the individual devices.

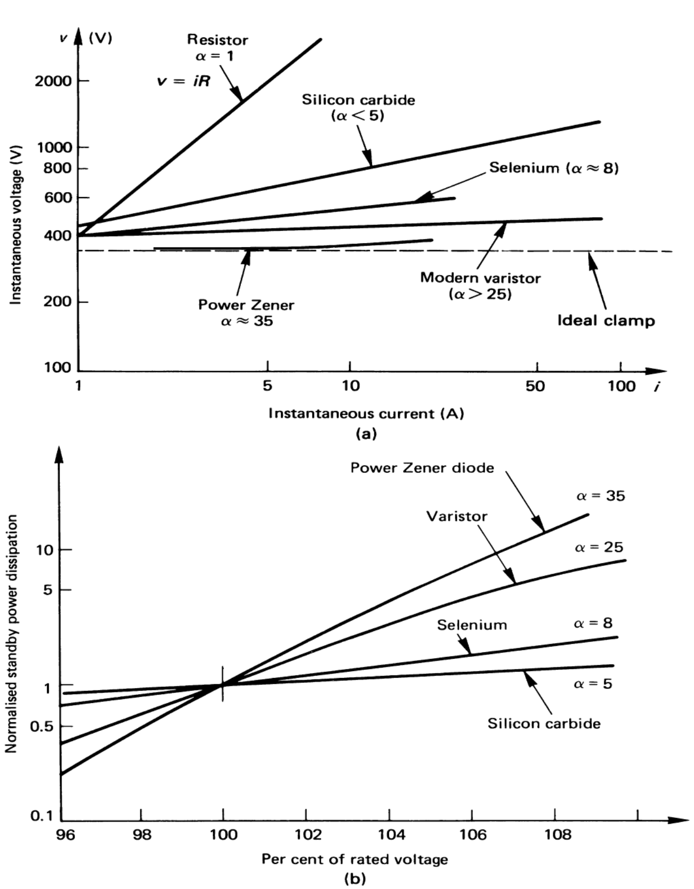


Figure 12.26. *(a) The I-V characteristics of four transient voltage suppressor devices, with resistance characteristics for reference and (b) standby power dissipation characteristics showing the higher the alpha the lower the standby power dissipation.*

Parallel operation is difficult and matched *I-V* characteristics are necessary.
A feature of varistors often overlooked is deterioration, which is not applicable to TVS diodes. Figure 12.27a shows that at relatively low energy levels an infinite number of transients can be absorbed, while at rated absorbed energy only one fault is allowed. This single fault, lifetime, is defined as that energy level that causes a 10 per cent increase in clamping voltage level, for a specified current density.

Figure 12.27b shows that high currents can be tolerated for short intervals. The lower the pulse repetition number, the higher the allowable current. The absorbed energy rating is given by

$$W = k\hat{I}\,V_c\,t_p \qquad \text{(J)} \qquad (12.25)$$

where k = 1 for a rectangular pulse and $k = \surd 2$ for impulse waveforms: 10μs/1000μs shown in figure 12.27a and 8μs/20μs. The maximum allowable energy pulse is usually based on a 2ms current pulse of magnitude such that a 10% variation in clamping voltage results. Varistors rated for 1000V ac, 1280V dc at 1mA standby, are capable of clamping once, 2870J associated with an 80kA, 2ms pulse, and have a typical capacitance of 2nF at 25°C and 1kHz.

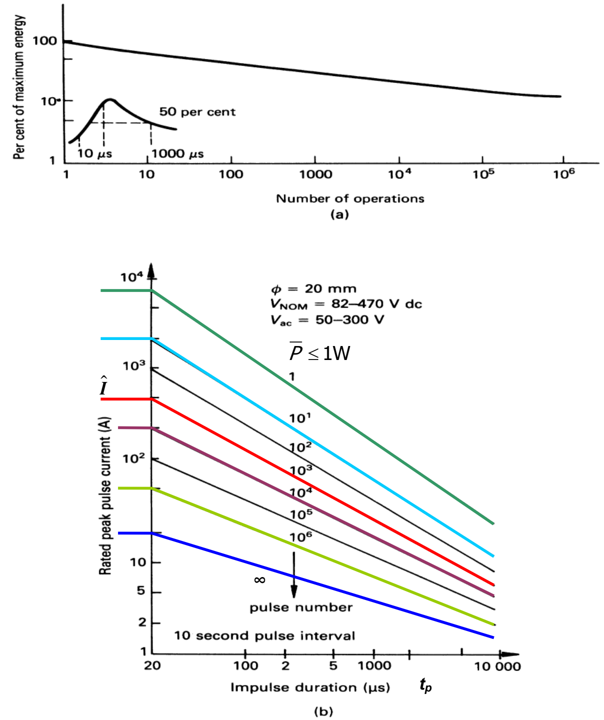


Figure 12.27. *Pulse lifetime ratings for a Zinc oxide varistor: (a) lifetime for fixed 10/100μs pulses and (b) lifetime number for variable-duration square-wave pulses.*

The failure mode of the Zener diode and varistor is a short circuit. Subsequent high current flow may cause an explosion and disintegration of contacts, forming an open circuit. This catastrophic condition can be avoided by fuse protection. Semiconductor based devices deteriorate minimally.

Table 12.5: Comparison of typical transient suppressor characteristics

Suppressor type	Standby current	Peak current at 1ms exp.	Peak power at 1ms	Peak energy	Voltage clamping ratio at 10A	Voltage range	Capacitance at 1MHz
	mA	A	kW	J		V dc	nF
Silicon carbide varistor	5	-	-	50	4.6	15-300	-
Selenium	12	30	9	9	2.3	35-700	-
Metal oxide varistor	1	120	40	70	1.7	14-1200	2
Zener diode (5W)	0.005	5.5	1.5	2	1.4	1.8-280	1

Selenium suppressors
Selenium, a naturally occurring substance, has been used as a semiconductor in rectifiers and suppressors. Although its popularity as a rectifier has virtually ceased in favour of its silicon equivalent, demand for selenium suppressors continues.
Depositing the elements on a metal substrate's surface produces selenium cells. This provides the cells with good thermal mass and energy dissipation as well as 'self-healing' characteristics, allowing the device to survive energy discharges in excess of the rated value. Selenium's crystalline structure gives it the ability to continue functioning after a burst of energy in excess of its short pulse width rating. Its

suppressor operation is comparable to a pressure relief valve – when the pressure rises, the relief valve opens, releases the pressure, and then resets itself.
Because of its unique properties, the selenium suppressor remains viable in many applications. Its transient voltage clamping characteristic, its ability to continuously dissipate power and handle long surges, make it better than MOVs or silicon suppressors for some applications.

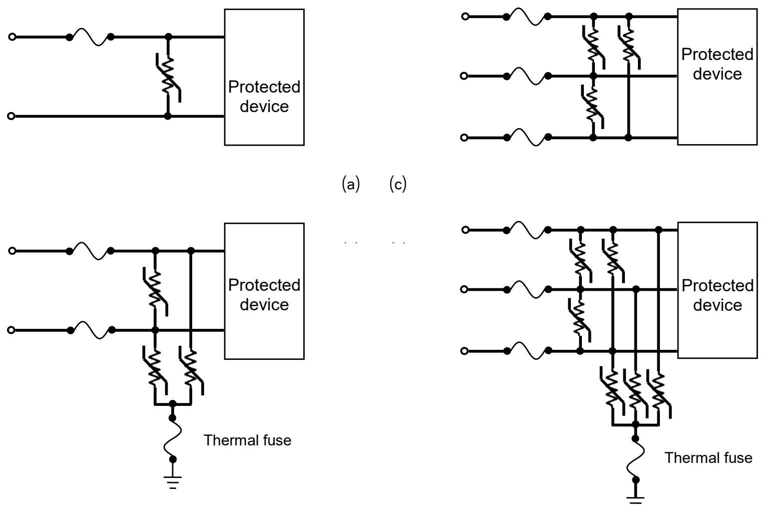


Figure 12.28. *Thermistor circuit protection: (a) ac single-phase or dc circuit protection; (b) ac single-phase circuit with line-line and line-ground protection; (c) ac three-phase circuit line-line protection; and (d) ac three-phase circuit with line-line and thermally fused line-ground protection.*

The selenium suppressor can absorb energy levels in excess of its rated capability while maintaining its clamping characteristics subsequent cycles. The layering of the suppressor onto the aluminium plate allows the suppressor's energy capabilities to follow that of a heat sink thermal curve. This heat sink capability allows steady-state power dissipation up to 40 times that of an MOV. For a 130V suppressor, the selenium suppressor allows steady-state dissipation of 2.5W to 80W, compared with an MOV that allows only 0.1W to 2.5W.
Selenium suppressor cell plates are available in sizes varying from less than 20mm x 20mm to in excess of 30mm x 30mm that can function at a temperature of 0°C to 55°C ambient without any derating. The voltage of a selenium suppressor cell starts at 26Vrms or 22.5Vdc per cell plate, with a 75V maximum due to the dielectric ceiling of the cell. The capacitor plate nature allows placement in series to attain higher voltage levels.
Other suppressors can handle high current, short pulse widths in the microsecond range, but the selenium suppressor can handle milli-second pulse width currents, making it a slower but a more robust suppressor than silicon devices. It has a typical response time of less than 1ms and is capable of handling pulses with long decay times as experienced with the shunt fields of large DC motors or any inductive loads with *L/R* ratios in the 100ms range, such as with power conditioning systems (that is, from power strips to a service entrance), generators, AC controllers, on the DC side of a rectified generator output, across SCRs on large controllers, and on transformers for line-to-line transient suppression.

Fundamentals of overvoltage protection theory
Electronic equipment and components have been designed to function properly when used within their specified current and voltage ratings. When these ratings are exceeded during operation, the equipment or components may sustain permanent damage and may cease to operate. Common sources of overvoltage conditions are lightning, ac power contact, and power induction. Other electrical components may be susceptible to shifts in system ground potential, increasing the need for overvoltage protection. Voltage protection devices may be installed in parallel with the equipment or components to be protected. In the event of an overvoltage condition, protection devices switch rapidly from a high to a low impedance state, thus clamping the transient voltage across the components to a safe operating level. Under normal operating conditions, the overvoltage device appears as a high impedance device (virtually open circuit, with minimal leakage current) and does not affect normal system operation.

Example 12.8: ***Non-linear voltage clamp***

Evaluate the current of a 1mA @ 250V Zener diode when used to clamp at 340V dc. At 340V dc, calculate the percentage decrease in voltage-dependent resistance and the per unit increase in power dissipation, assuming $\alpha = 30$.

Solution

i. From $I = kV^{\alpha}$, equation (12.20)
$I_2 = I_1(V_2/V_1)^{\alpha}$ = 1 mA (340V/250V)^{30} = 10.14A
The Zener diode will conduct 10.14A when clamping at 340V (a 10,140 increase on the standby current of 1mA)

ii. From equation (12.22), $R = V^{1-\alpha}/k$ therefore

$$1-\frac{R_2}{R_1}=1-\left(\frac{V_2}{V_1}\right)^{1-\alpha}=1-\left(\frac{340\text{V}}{250\text{V}}\right)^{-29}=0.99987$$

The percentage decrease in resistance is 99.987 per cent.
The static resistance decreases from (250V / 1mA) 250kΩ to (340V / 10.1A) 33.5Ω.
By differentiating equation (12.20), the incremental resistance (*dv/di*) reduces to 1.12Ω (33.5Ω/30).

iii. $P = kV^{\alpha+1}$ (equation (12.24))

$$\frac{P_2}{P_1}-1=\left(\frac{V_2}{V_1}\right)^{31}-1=\left(\frac{340\text{V}}{250\text{V}}\right)^{31}-1=13793.5$$

The per unit power increase is 13,800.
The power increases from (250V × 1mA) 0.2 W at 250V standby to (340V ×10.14A) 3447.6 W when clamping at 340V dc.

♣

12.3.2 Transient voltage fold-back devices

A fold-back device is normally in a high-resistance state for voltages below the break-over voltage. In this state little current flows through the device. When the voltage exceeds the break-over voltage, the device *folds back* or goes into a low-impedance state, allowing the device to conduct large currents away from sensitive parallel connected electronics. The device will continue to remain in this low impedance state until the current through the device is decreased below its holding current.

Fold-back devices have an advantage over clamping devices because in the fold-back state little voltage appears across the load while the device conducts harmful surges away from the load, whereas clamping devices remain at the clamping voltage. The power dissipated in the fold-back device is therefore much lower than in a clamping device, allowing a much smaller device to be used to conduct the same amount of surge current. In addition to its smaller size and lower power dissipation, a fold-back device offers lower capacitance and cost for a given silicon die area.

12.3.2i The surge arrester

A surge arrestor (or gas discharge tube, GDT) is a high-current, two terminal, hermetically sealed-gas (usually neon and argon) discharge element, as shown in figure 12.29. GDTs apply a short circuit under surge conditions, returning to a high impedance state after the surge. The sealing shields the device from external impregnation, hence ensuring stable gas-physics properties. The internal electrodes are especially electron emission promoted coated for stability and are displaced by about 1mm. The inner cylindrical surface of the insulator is ignition-aid coated to speed-up and stabilise the gas discharge, by distorting the electric field. These features define the electrical characteristics such as spark-over voltage, low capacitance, pulsed and ac discharge current handling capability, as specified in figure 12.30.

Unlike the varistor or Zener diode, the voltage collapses to near zero when the external surge voltage exceeds the device internal electric field strength, eventually creating an low voltage (10V) sustained ionised arc, which is only extinguished when the external energy is reduced to zero, as resulting from a voltage reversal in an ac circuit.

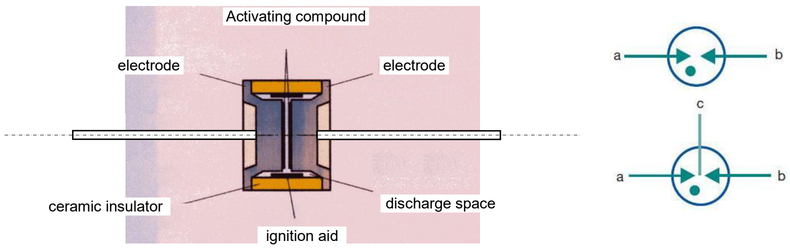


Figure 12.29. *Construction of an inert gas surge arrestor and 2 and 3 electrode GDT circuit symbol.*

A number of transitional stages occur during surge voltage suppression, as shown in figure 12.30.

- When inactive, the surge arrestor appears as a low capacitance (<1pF) in parallel with a high resistance, typically 1GΩ, where virtually no current flows.
- When the element *spark-over voltage* is reached, V_s (devices ranging between 70V and 5kV). The voltage rapidly falls to the *glow voltage level* V_{gl}, which is between 70 to 200V with a low current of 10mA, gradually increasing to about 1.5A – region G in figure 12.30.
- As the arrestor current increases, transition to the *arc voltage* V_a mode occurs, where the voltage falls to 10V to 35V, independent of the subsequent current – region A. The transition time between the glow and arc region is dependent on the available current of the impulse, the distance and shape of the electrodes, the gas composition, gas pressure, and the proprietary emission coatings.
- As the over-voltage decreases, the arrestor current decreases to a level where the arc cannot be sustained. The arc ceased suddenly, passing briefly through the glow region, and finally extinguishing at the voltage V_e, termed the *extinguishing voltage*.

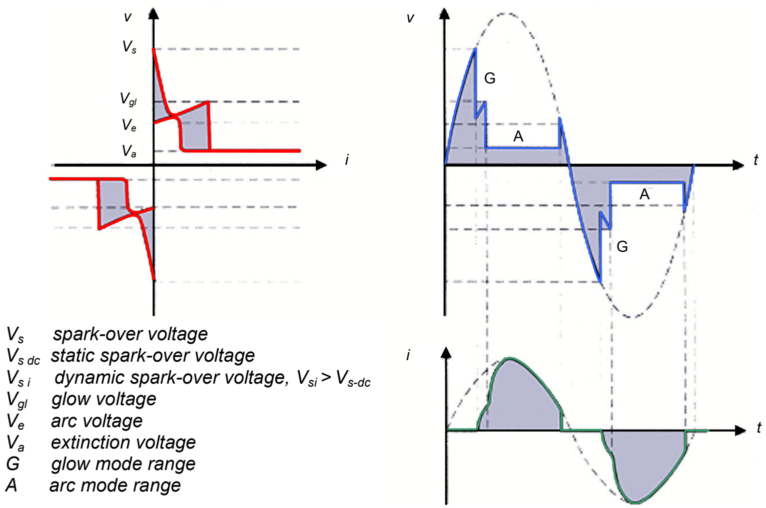


Figure 12.30. *Over-voltage limiting characteristics of an inert gas surge arrestor.*

Response behaviour

The rate of rise of terminal voltage affects the electrical performance, as shown in figure 12.31a. At low *dv/dt*'s (<1V/µs), the *dc spark-over voltage* $V_{s\text{-}dc}$ of ignition is determined by the electrode spacing, the gas type and pressure, and the degree of pre-ionization of the noble gas.

At high *dv/dt*'s, the spark-over voltage exceeds the lower steady-state value, $V_{s\text{-}dc}$. The ignition-aid coating on the inner cylindrical surface reduces the voltage spread of the resultant *impulse spark-over voltage* $V_{s\,i}$. GDTs have no *di/dt* sensitivity.

The operating mechanisms are such that the surge arrestor is not normally suited to dc-circuit operation (or highly inductive ac loads), since to revert to a high impedance mode, the current must drop below the arc discharge mode minimum level of a few 100mA. For this reason, a fail-safe mechanism is incorporated to expend the resultant high heating losses that occur with continuous arcing. A spring tension-loaded thermal fuse type mechanism is incorporated to short the two electrodes after melting the separating insulating spacer. Figure 12.31b show the typical short-circuit reaction characteristics as a function of the current flowing through the arrestor.

Switching spark gaps

The gas discharge principle used in the voltage surge arrestor is also applicable to the three-terminal switching spark gap, figure 12.29. The device is deliberately ignited, by the build-up of the terminal voltage, (devices from a few hundred volts, up to 6kV) to produce extremely fast (<50ns) high current (>1kA) switching operations (>2M operations), over a very wide temperature range, virtually without loss when conducting and a high insulating resistance (>100MΩ) when non-conducting.

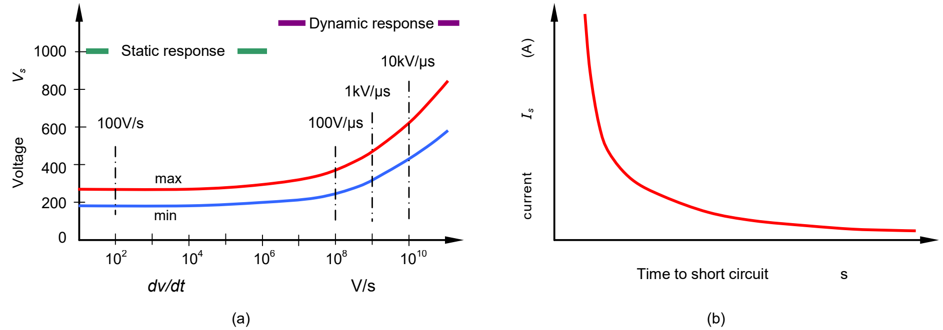


Figure 12.31. *Surge arrestor dynamic characteristics: (a) dv/dt response and (b) fusing time.*

The Dark Effect

The first surge on the GDT tube results in a higher breakdown than subsequent successive surges. As the GDT is normally housed in a plastic module and deployed in a dark cabinet, the term was called the dark effect. The initial strike ionizes the gas to make it settle into a consistent breakdown voltage specification. The impact has been reduced by the design geometry and emission coating composition of the gas tube. The first surge impulse is typically 10% higher than the average impulse let-through voltage. Surge at very high impulse current levels do not experience the phenomenon, which indicates the dark effect is dependent on the surge current and source impedance.

The Spark Effect

The spark effect is due to the arc being of a high enough energy density to cause contaminants (impurities) to be released from the internal materials into the GDT gas atmosphere under a single surge. These contaminants in the gas cause the increase of the dc breakdown voltage by more than 10% between the first two surges. Subsequent surges trigger the 'getter' effect of the emission coating that will attract the impurities (contaminants) and reduce the breakdown voltage to the original level. Contaminants suspended in the gas change the gas composition and decrease or increase the breakdown voltage according to the Paschen curve of the particular gas mixture.

GDT Life Cycle

The GDT does wear out due to particulates being dislodged from the electrodes during tube arcing. The impact of the arc across the tube is dependent on the energy strike, so the life of the GDT tube is dependent on the impulse applied to it.
The surge ionizing effect charges the tube and therefore attracts the particulates to one end of the tube. This has the effect of changing the electrical properties such as the dc breakdown voltage.
The end of life shorting of the GDT is caused by the rapid breakdown of the emission coating and the electrode material (metal) that further increases internal contaminates. The free materials in the tube attach themselves to the side of the ceramic body between the two electrodes, thereby causing a 'virtual short' between the electrodes.

12.3.2ii Thyristor voltage fold-back devices

Thyristor-based devices initially clamp the line voltage, then switch to a low-voltage on-state. After the surge, when the device current drops below its 'holding current', the protecting device returns to its original high impedance (off) state.

Figure 12.32 shows the protection action difference between a device that voltage clamps (diode avalanche breakdown action, figure 12.32a), and a device that initially clamps then voltage folds back to a low impedance state (thyristor action, figure 12.32b). The main benefits of thyristor type protection are lower voltage overshoot and an ability to handle moderate currents without device wear-out or a deterioration mechanism. The disadvantages of thyristor protectors are relatively high capacitance, which is a limitation in high-speed digital applications, and low tolerance of excessive current. Thyristor circuit protectors can act either as secondary protection in conjunction with gas discharge tubes, GDTs, or as primary protection for more controlled environments of lower surge magnitudes.

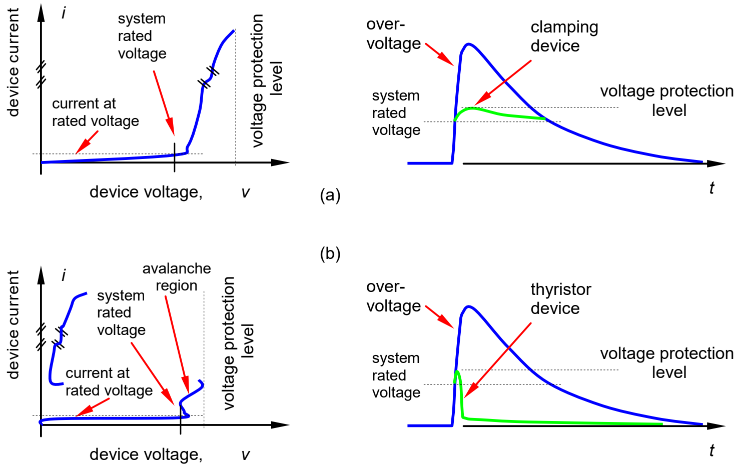


Figure 12.32. *Semiconductor I-V characteristics and switching voltage performance: (a) clamping and (b) fold-back devices.*

Thyristors are multilevel layers of n and p doped silicon which form regenerate connected bipolar transistors. When the bipolar transistors are triggered they can enter into a self-sustaining low-resistance state. Thyristors, specifically the SCR, is inherently a unidirectional crowbar device. Modifications of the basic SCR have produced a variety of bidirectional and unidirectional options, specifically the triac and diac (diode for alternating current), as shown in figure 12.33.

The protection capability of an SCR is asymmetrical as shown in Figure 12.33a. In the positive direction, turn on of the thyristor results in a dramatic decrease in resistance while in the negative direction the thyristor provides voltage clamping action, similar to a diode based TVS device. For protection in both voltage polarities, to provide symmetrical crowbar behaviour, it is necessary to use two anti parallel SCRs. This can be achieved with a pair of discrete SCRs, or with an integrated structure in a single silicon die that has five doped regions, as illustrated in Figure 12.33. The integrated device is usually called a Thyristor Surge Protection Device (TSPD) and its *I-V* characteristic is shown in Figure 12.34a. The clamping voltage level of fixed voltage thyristors is set during the manufacturing process. Gated thyristors have their protective level set by the voltage applied to the gate terminal.

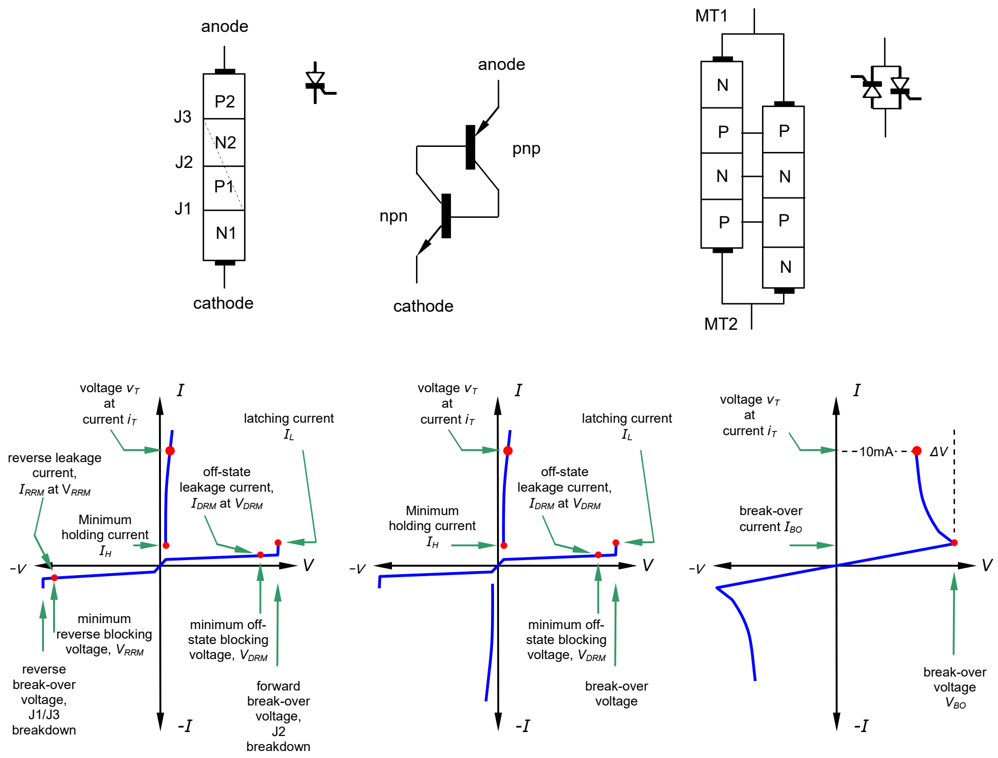


Figure 12.33. *Thyristor physical structure, equivalent circuit and I-V curves for thyristors: (a) an SCR; (b) a pair of anti-parallel SCRs, the triac; and (c) the diac.*

In response to a transient surge, the thyristor voltage folds back to provide a low-impedance path to ground. The circuit must have enough impedance to limit the fault current below the peak pulse current (I_{PP}) rating of the thyristor. The over-current protector typically does not operate during a lightning pulse. Two voltage triggered fold-back silicon semiconductor devices are commonly used for circuit voltage protection, the thyristor surge protection device, TSPD, and the SIDAC (silicon thyristor (diode, misnomer) device for alternating current). Both are voltage triggered switches but the TSPD is used to reliably protect telecom lines from high current levels and over-voltage occurrences while a SIDAC (a more electrically robust DIAC) is intended for use as a triggering device.

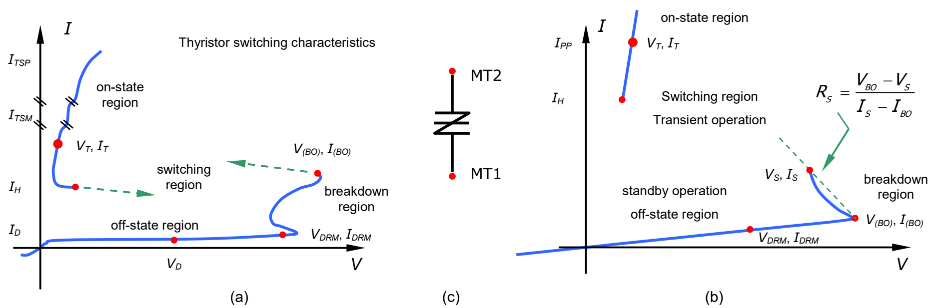


Figure 12.34. *Thyristor fold-back I-V operation: (a) TSPD; (b) SIDAC; and (c) circuit symbol.*

The TSPD

The TSPD is a silicon structure device typically manufactured on an n-type substrate. It is the equivalent of two SCR's 'connected' in anti-parallel, which allows the flow of electric current in both directions. The TSPD is capable of sinking a surge current pulse to ground when transient voltage appears across its two terminals, occurring when the break-over voltage of the device is reached. The device typically operates symmetrically, protecting in the positive and negative direction. The TSPD turns from the off-state to the on-state based on the breakdown and break-over voltage levels that appear between its two terminals, MT1 and MT2. The devices have a current and voltage curve that has a 'fold-back' affect, where the break-over is high, while the clamping voltage is low, basically a short, after the device turns-on giving it high surge abilities. Figure 12.34c shows the symbol for both the TSPD and the SIDAC.

The TSPD is a crowbar device, meaning it has two states of functionality: open circuit and short circuit. It is transparent during normal circuit operation, in that it is an open circuit across its two terminals. Most TSPDs are symmetrical bidirectional designs but there are also unidirectional devices with a built in diode, or asymmetric bidirectional TSPDs are available with a reduced break-over trigger voltage in one polarity.

Typical TSPD surge current capabilities are up to 200A for a 10/1000μs surge voltage. Operating voltages typically cover a broad range, from 12V up through several hundred volts. They have good *dv/dt* sensitivity but poor *di/dt* sensitivity.

The main features of TSPDs are:

Advantages:

- There is no wear–out (ageing) mechanism present as with GDTs and MOVs
- Very fast turn-on switching
- Electrical parameter consistency (V_{BO}, V_{BR}, I_H)
- High immunity to *dv/dt* conditions (>2kV/ms)
- Compared with the MOV, the total energy dissipated is lower, since the crowbar characteristic is not possessed by MOV devices
- Similar current surge capabilities as the GDT
- Short circuit mechanism for protection of the equipment

Disadvantages:

- Very high current surge pulse limitation, where more silicon is needed
- Temperature dependency of the electrical parameters
- Surge performance limited at low temperatures (< -20°C)
- Capacitance is dependent on the die size, but lower than TVS

The SIDAC

The SIDAC is a multi-layer silicon semiconductor usually manufactured on a p-type substrate. Being a bilateral device, it switches from a blocking state to a conducting state when the applied voltage of either polarity exceeds the break-over voltage. As with other trigger devices, the SIDAC switches through a negative resistance region to the low voltage on-state and will remain on until the main terminal current is interrupted or falls below the holding current. When the SIDAC switches to the on state, the voltage across the device drops to less than 3V, depending on magnitude of the main terminal current flow. The main application for the SIDAC is ignition circuits or inexpensive high voltage power supplies.

The difference between a TSPD and a SIDAC is that the SIDAC is intended to be used as a triggering device. The TSPD is intended to withstand surge current levels which involves high levels of peak power, such as required by telecommunication protection standards. Most of the applications for the SIDAC's are related to capacitor discharge circuitry, as part of a *RLC* circuit; commonly as lamp starters, strobes and flasher, a stove igniter, etc. The key features of the SIDAC are similar to those of the TSPD. When comparing a similar TSPD with a SIDAC device, the surge current abilities of the TSPD are much larger than the SIDAC. Other key parameters that TSPDs advantageously have over SIDACs are lower leakage current (I_{DRM}) and *dv/dt* immunity.

The I-V curve in figure 12.34b shows the electrical characteristics of a SIDAC. Typical devices are rated at 1A, 220V with junction operating temperatures up to 125°C. Commutation times are better than 100μs and the switching resistance R_s in figure 12.34b, is typically 100Ω.

12.3.2iii Polymeric voltage variable material technologies

Polymer Electrostatic Discharge (ESD) suppressor devices consist of a polymer embedded with conducting particles as shown in Figure 12.35a. At high voltage, arcs between the particles create a low resistance path resulting in a drop in voltage. Additionally, the polymeric suppressors can be manufactured with a gap in an electrode that connects two end terminations. The gap causes the two terminations to be electrically discontinuous (current cannot flow). Into the gap, a polymer-based material is back-filled. This voltage variable material (VVM) has similar electrical characteristics to zinc-

oxide material. Under normal circuit conditions, the VVM acts like an insulator, but when an ESD transient occurs, the VVM transits to a conductor and shunts the ESD to ground. Polymer devices are bidirectional crowbar devices as shown in Figure 12.35b.

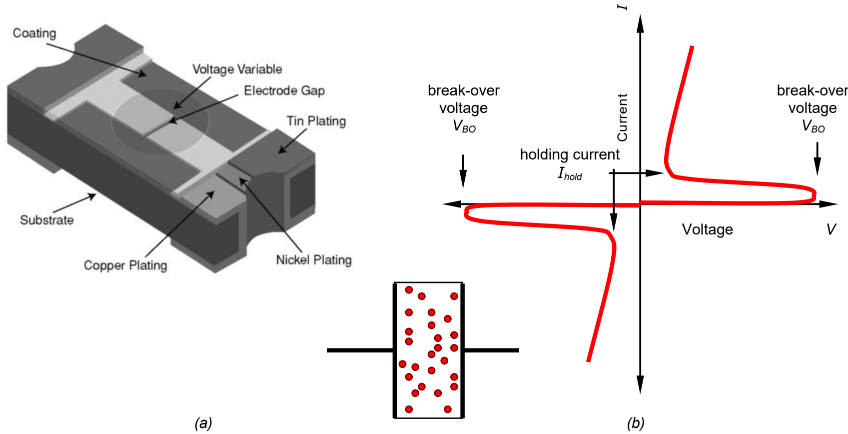


Figure 12.35. *Polymer ESD suppressor: (a) construction and (b) I-V curve of a polymer device.*

Polymer ESD suppressor devices are specifically for electrostatic discharge protection of sensitive low voltage technology. ESD is the transfer of electrical charge between any two objects. ESD is different from other, common overvoltage events (switching and surge transients) in that the time it takes ESD to transition from zero to maximum current and voltage is very short. The rise time of an ESD event is less than a nanosecond, while the other transients take longer than a microsecond to reach their peaks. Since polymeric suppressors are generally specifically designed only for ESD protection, they are not capable of withstanding the higher energy levels of surge transients. On the other hand, polymeric products have the lowest capacitance, 0.050pF, of the suppressor technologies and are used to protect high-speed communication lines.

Polymer devices have high bipolar turn-on voltages, usually over 100V, but turn-on quickly, limiting the exposure to high voltage. The working voltage ranges up to 24V dc, with a leakage current of less than 1nA. The operating temperature range is typically from -65°C to +125°C.

Differences between the GDT and the solid-state semiconductor TSPD thyristor

Static spark-over voltage $V_{s\text{-}dc}$ versus repetitive peak off-state voltage, V_{DRM}

Both define the maximum working voltage across the protector before conduction occurs where the protector will have high impedance so that it will not interfere with the normal operation of the system. The DC surge voltage $V_{s\text{-}dc}$ is specified as a typical voltage where the tolerance has to be used to define the minimum rating to not interfere with system's operating voltage. The TSPD thyristor V_{DRM} is specified as an absolute maximum in its data sheets. The DC surge voltage $V_{s\text{-}dc}$ is measured by using a slow ramp voltage such as a 100 V/s to 2000 V/s. The V_{DRM} for the TSPD thyristor is measured at a specific current value and is specified as a maximum of 5 μA at the V_{DRM} value.

Impulse spark-over voltage versus dynamic breakover voltage, $V_{(BO)}$

Both define the maximum dynamic protection voltage window of the protectors. The protection voltage is the maximum voltage the system will see. The GDT impulse voltage and the $V_{(BO)}$ impulse breakover voltage of a TSPD thyristor are specified at a ramp voltage of 100 V/μs or 1000 V/μs. The TSPD thyristor has a tighter maximum working voltage to protection voltage (V_{DRM} /$V_{(BO)}$) window.

Impulse discharge current versus non-repetitive peak impulse current

These two parameters highlight the surge withstand rating of the protector where both are specified using industry standard surge waveforms. The GDT will specify a short circuit current level and the minimum number of operations it can withstand. Although the GDT has much higher impulse surge ratings, the TSPD thyristor does not have a wear-out mechanism like the GDT, so its impulse current ratings are specified as an absolute maximum.

Capacitance

Capacitance of a GDT (typically 2pF) is significantly lower than a TSPD thyristor (hundreds of pF). The capacitance of a GDT is not affected by any bias or signal voltages across it and does not change with temperature. A TSPD thyristor or any semiconductor overvoltage protector will have a capacitance dependent on the surge rating (which is dependent on silicon size) and will change according to the bias voltage across it. Thyristor capacitance will also vary with the protection voltage of the same surge rating series, where low V_{DRM} voltage options will have a higher capacitance value.

12.3.2iv The crowbar

A *crowbar* can be used for overvoltage and/or over-current protection in both ac and dc circuits. Figure 12.36 illustrates how an SCR can be used to provide fault protection for sensitive dc power electronic circuits and loads. Whenever a fault condition occurs the crowbar SCR is triggered, shorting the supply. The resultant high supply current blows the fuse, or initiates a fast-acting circuit breaker/mcb, thereby isolating the load from the supply. The diode D_c provides a current path for inductive load energy.
The load current is measured by the voltage across the sense resistor *R*. When this voltage reaches a preset limit, that is the load current has reached the fault level, the SCR is triggered. The load or dc link voltage is measured from the resistor divider R_2 - R_3. When this voltage exceeds the pre-determined limit the SCR is triggered and the fuse is blown by the crowbar short-circuit current, isolating the sensitive load from the supply. The load voltage is safely clamped to zero by the conducting SCR or diode D_c.
A judiciously selected crowbar SCR can conduct many times its average current rating. For the few milliseconds in which the fuse is isolating, the SCR I^2t surge current feature can be exploited. The SCR I^2t rating must be larger than the fuse total I^2t rating. If the SCR crowbar is fuse-link protected then the total I^2t of the dc-link fuse link must be less than the pre-arcing I^2t of the SCR crowbar fuse link.
An ac crowbar can comprise two antiparallel-connected SCR's across the fuse-protected ac line, or alternatively one SCR in a four-diode full-wave rectifying bridge.

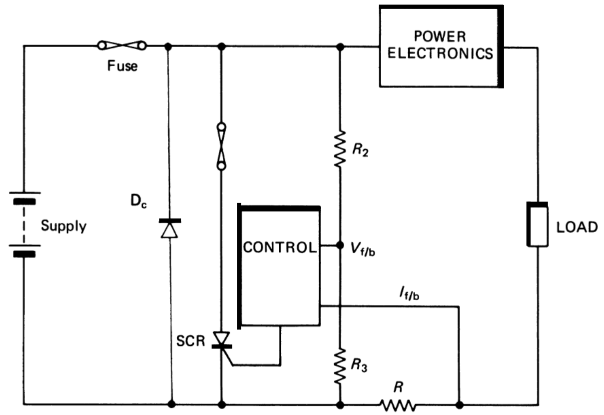


Figure 12.36. *An SCR crowbar for overvoltage and over-current protection.*

12.3.3 Protection coordination

Some primary protective devices such as semiconductor-based devices are fast enough to react in time; however these devices tend to have limited current handling capability. Also, semiconductor devices rated for the primary protection task tend to capacitively load a circuit (due to their physically large size) resulting in bandwidth limitations. Non-semiconductor surge protectors, such as the Gas Discharge Tube (GDT), do not capacitively load circuits and can handle very large currents (tens of kA); however, these devices are slower to react and may not keep the voltages sufficiently low to provide successful protection by themselves. Therefore, conventional protection must be based on a number of stages of such devices. These stages typically start with a GDT as the primary protector for its current handling capability, followed by a semiconductor thyristor protector for speed – the secondary protector.
When GDT and thyristor shunt protectors are used as primary and secondary protectors, the protection coordination between them is complicated in practice. When a surge event occurs, the fast secondary protector will act to limit voltage within the system first (due to its speed). Often this protector will be rated to keep the circuit voltages quite low in order to protect the equipment. Thus, its action can prevent

the high energy primary protector (GDT), which requires a higher voltage to operate, from working. In this circumstance, damage is likely to occur to the secondary protector before the GDT operates.
This problem is solved by the complex process of inter-stage coordination. Coordination is the process of placing impedance between the primary and secondary protectors to ensure that sufficient voltage is generated across the primary protector, resulting from current flowing in the secondary protector, to trigger the primary device. Coordination is engineered properly when the primary protector operates after the secondary protector operates, yet before the secondary protector is damaged. The coordinating impedance can be resistive, capacitive, inductive, non-linear or a combination of all of these; proper selection is critical.
Large resistance is the easiest choice to ensure that only a small current in the secondary device causes a significant voltage across the primary device causing it to operate. However, large resistance introduces considerable loss within the transmission path which is often unacceptable. Capacitance and inductance are also useful, but these impedances are frequency related and so circuits coordinated with such will function only for a band of surge frequencies. Non-linear resistance can also be used to create different coordinating arrangements based on the duration of the surge - low level surges for example which last a long time causing the coordinating impedance to change to a high resistance state choking further current flow and triggering the primary protector (the basis of operation of the PTC).

12.3.4 Summary of voltage protection devices

There is a variety of devices available to provide shunt electrical over-voltage protection to electronic systems and components. Each device has its own *I-V* characteristics as in figure 12.37 and Table 12.6.

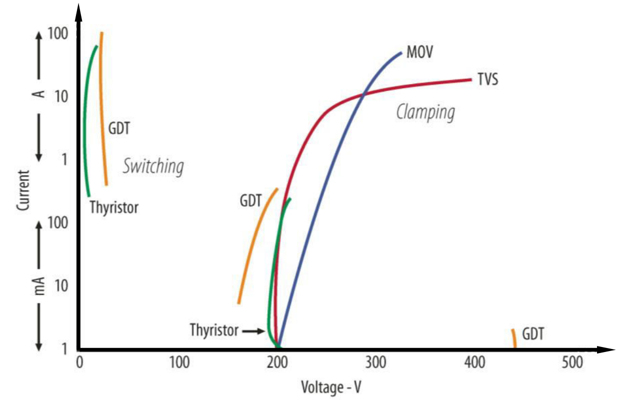


Figure 12.37. *The different I-V characteristics of over-voltage protectors.*

Table 12.6: Features of various protection device technologies. **All reset to normal after operation**

ype	Protection Mechanism	Polarity	Clamp or Crowbar	Speed	Voltage Accuracy	Current Capability	Size / Capacitance	Lowest Trigger Voltage	deterioration
High Power Surge Events – 8/20 μs, 10/1000 μs, etc.									
Gas Discharge Tube GDT	Breakdown of a gas at high voltage	Bidirectional	Crowbar	Slow	Fair	Very high	Large / low	75V	No, depends on severity
Thyristor Surge Protection Device TSPD	Turn on of coupled bipolar transistors - thyristor	Unidirectional or Bidirectional	Crowbar	Fair	Good	Medium to high	Small / medium	80V	No
Transient Voltage Suppressor TVS	Forward bias and reverse bias diode conduction	Bidirectional	Clamp	Fast	Good	Low	Small / high	NA	No
Metal Oxide Varistor MOV	Non-linear resistance of ceramic of zinc oxide grains	Bidirectional or Unidirectional	Clamp	Fair	Poor	Medium to High	Small / medium	NA	Yes
Very Fast Surge Events – ESD									
Polymer ESD Device PESD	Arcing between particles in polymer	Bidirectional	Crowbar	Fast	Poor	Low	Small / low	~100V	Yes

Overvoltage protection technologies may be summarized as follows:

- GDTs offer the best AC power and high surge current capability. For high speed systems, the low capacitance makes GDTs the preferred choice.
- Thyristors provide better impulse protection, but at a lower current.
- MOVs are low cost components, with modest performance properties.
- TVS offers better performance in low dissipation applications.

12.4 DC Circuit Breakers

DC circuit breaker, DCCB, requirements, although application dependant, include voltage and current ratings, plus energy to be absorbed, and importantly, operational speed.

The basic DCCB approaches are:

- Purely semiconductor
- Hybrid - mechanical breaker plus semiconductor
- Functionality unification – main converter with dc block capability

Generally resonant approaches are not favoured because of the high resonant circuit voltages and currents, which are in excess of the already stressed system operational levels.
Purely mechanical contact based dc circuit breakers are considered in Chapter 33.11.

12.4.1 Purely semiconductor DCCB

With no moving parts, the operating speed of series connected semiconductor switches, as shown in figure 12.18a, far exceeds the capability of conventional mechanical circuit breakers. If the short circuit current can be quickly detected, a semiconductor circuit breaker is capable of isolating the circuit in tens of microsecond. Therefore the let through fault current would be limited with less possibility of damage to equipment.

An IGBT in series with a diode is needed for bidirectional voltage blocking whilst an IGBT in anti-parallel with a diode is needed for reverse current capability, as shown in figure 12.38c. Operation within 20μs is viable, so the pulse rating of the IGBT (double the nominal current for 1ms) can be exploited during the fault clearing period.

The inevitable extensive device series connection results in high continuous conduction losses during the on-state. There are no major switch synchronisation problems at turn-off of the series device string, since each device is shunt protected and voltage clamped by an MOV. Also IGBT turn-off can be staggered (stepped) to prevent and control the voltage collapse/rise tendency of the dc link each side of the DCCB (voltage change depends on the direction of current relative to the node and fault). Shunt MOVs across the dc link are needed each side of the DCCB to limit link/cable/line over-voltages.

Example 12.9: ***IGBT DC circuit breaker***

Determine the semiconductor requirements for a ±400kV, 1500A semiconductor DC circuit breaker. The applicable semiconductor I-V characteristics are given within the solution.

Solution

i. For 1500A, two parallel 6.5kV, 750A IGBTs plus diodes yield 3.7V+3V=6.7V on-state, giving 6.7Vx1.5kA=10kW on-state losses (about 5kW per 12kW rated semiconductor package). IGBTs rated at 6.5kV would be matched with MOVs that clamp 2kA at 6kV (4kV steady-state stand-off).

The result is an on-state voltage of 1.7V/kV, that is, the DCCB on-state voltage is 670V, 0.17% (100 series IGBT/diode) on a 400kV link. Therefore 200 igbts and 200 diodes are required for bidirectional functionality (±400kV).

ii. A feature of a semiconductor DCCB is that the diodes do not require fast recovery properties. Rectifier grade diodes would offer a reduced diode voltage of 1.4V at 2kA, as opposed to 3V at 1500A. At 400kV, the on-state voltage decreases from 670V to 510V (0.13%), meaning continuous on-state losses decrease from 1MW to 765kW (in a 600MW unipolar system, ≈0.1%). This is 2kW/kV at 1500A.

♣

12.4.2 Hybrid DCCB: semiconductors shunted by a circuit breaker

The high on-state losses of a semiconductor DCCB can be mitigated by a hybrid approach of semiconductors in parallel with a mechanical circuit breaker, as shown in figure 12.38. The fault clearing time is compromised.

The concept is based on expired patent US 4636907A, 1987, The main series string T_{shunt} is always first on and last off. Confined to these timing constraints, the auxiliary switch T_{gap} controls the CB such that it only conducts after the gap is closed and ceases conduction before being opened. Figure 12.38 parts b and d show unidirectional and bidirectional hybrid DCCBs.

In hybrid circuit breakers, contact turn-on problems (bounce, arcing, etc.) are minimal, since the shunt semiconductors T_{series} conduct first, and subsequently the contacts close at high current but low voltage. Additionally the initially inrush current (experience by the IGBTs) is usually controlled by a series saturable reactor L_s, which limits the initial *di/dt* and rise of the fault current. An advantage of this low energy contact closing procedure is the absence of contact welding, since contact closing does not involve significant contact material melting. The bypass CB and T_{gap} offer low on-state losses. CB turn-off arcing, etc. are avoided by the semiconductor T_{gap} being the current commutating element. The voltage rating of the single series switch T_{gap}, in conjunction with circuit stray inductance, determine how fast the current commutates from the CB to the series string (*v=Ldi/dt*).

Performance is dominated by mechanical vacuum circuit breaker characteristics (Chapter 33).

- Opening contact speed is at best 2m/s (closing is at 1m/s).
- Necessary gap distance depends on voltage, with 1cm for 15kV ac (5ms) and 3mm for 3kV (1.5ms). That is, the higher the voltage the longer the time to fully open the gap.
- Vacuum arc sustaining voltage is about 50-80V but can be as low as 25V (pole material is a second order factor). 300V for SF_6 and 500V for oil. (NB: onstate voltage $V_{Tshunt}<V_{arc\ sustaining}$)

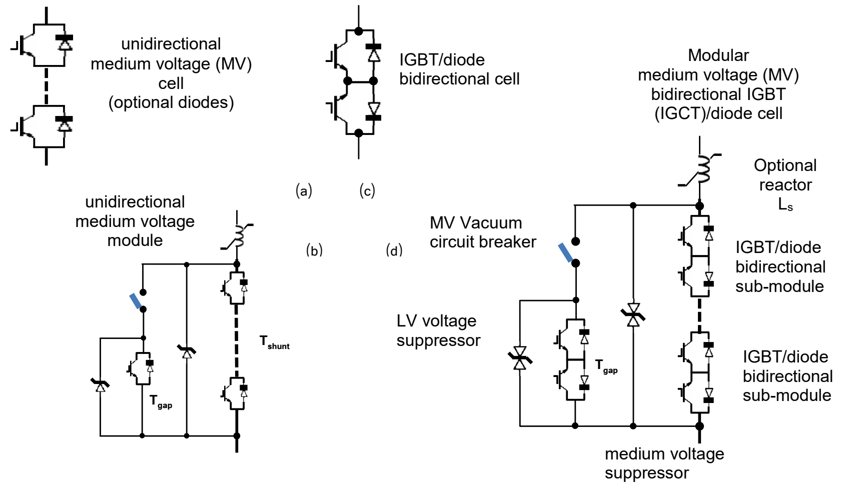


Figure 12.38. *DCCB semiconductor modules and cells for:*
(a) and (b) unidirectional operation and (c) and (d) bidirectional functionality.

While the CB in figure 12.39 is opening, the fault current rises through the high-voltage series semiconductor string T_{shunt}. The higher the circuit voltage the wider the necessary contact gap, the longer the opening time, the higher the developing fault current. Because the gap opening time is of the order of many ms, the IGBT T_{shunt} current rating requirement is high: much higher than the system continuous dc current rating. During this time the system dc voltage may collapse and propagate, meaning a system black start is required.

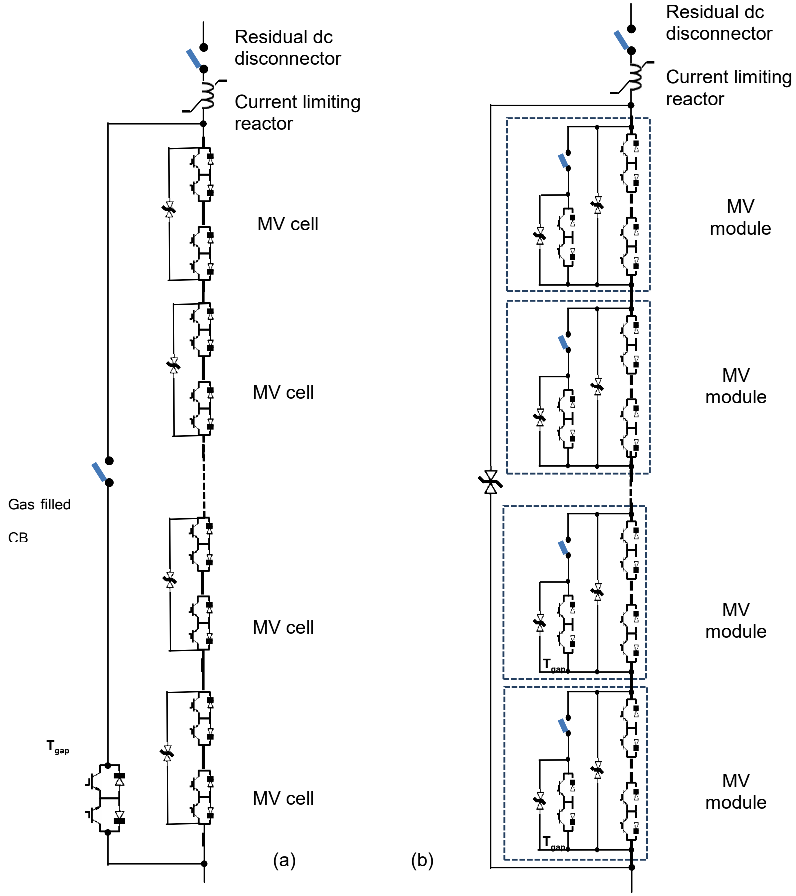


Figure 12.39. *Hybrid DCCBs.*

In some applications, it may be possible to eliminate the switch T_{gap}. Without T_{gap}, during contact opening arcing, a minimum gap voltage must exist for gap current to flow, so if the gap voltage can be suppressed below this level, the CB current will commutate. Effectively a voltage 'zero' is produced. Thus if many modules are used, with a VCB in each, as in figure 12.39b, without the switch T_{gap} in series with the CB, provided the on-state voltage of T_{gap} is less than about 50V, the arc will commutate to T_{shunt}. The time to commutate the current from the CB to the series string T_{shunt} is lengthy because the voltage produce to overcome the stray inductance is low, less than 50V.

Features of the approach in figure 12.39b, without T_{gap} (as opposed to figure 12.39a):

- redundancy: if a device failure is open circuit, the module VCB provides a bypass path
- fully modular structure
- low stray inductance because of compact commutation paths
- 15kV ac vacuum technology is possible
- no high voltage VCB arcing (above about 15kV, X-rays are produced)
- igbt T_{gap} losses occur in each VCB path in figure 12.39b
- transient recovery voltage, TRV, occurs at current chopping, necessitating voltage suppression
- AgWCu or CuCr type contact materials, with low chopping current (1A/4A), is mandatory

Features of the hybrid dc circuit breaker in figure 12.39a, which incorporates T_{gap}, are:

- no contact current when opened, resulting in virtually zero arcing and no transient recovery voltage, TRV, since no current chopping
- because zero current is broken, HV gas filled technology can be employed as a CB/disconnector.

- A high voltage (that of T_{gap}) is used to commutate the current from one path to another, thus short commutation times are possible when overcoming the effects of stray inductance
- Contact material can have a lower work function, Cu, hence lower flat/butt contact resistance
- Only one CB plunger so fewer lubrication dry-out problems (contact I^2R causes plunger heating)
- No need for synchronisation/matching//timing of multiple circuit breaker opening operation
- Leakage current of T_{gap} is well below chopping current level.

12.4.3 Functionality unification – main converter with dc block capability

Most ac to dc converters behave as uncontrolled rectifiers when the dc link has a short circuit, hence ac currents are only limited by transformer leakage inductance, which may be deliberately increased at the expense of loss of volts for VAr production. The ac side VCBs can protect the grid from the dc fault prospective currents levels, in about 33ms/40ms.

The switch and capacitor arrangement of the cascaded H-bridge converter (Chapter 17.3.3) can block the ac side from feeding a dc fault. The penalty is more semiconductor switches in each current path, hence higher losses. A fast DCCB is still needed at the other side of the dc fault, while the dc fault blocking capability of the main ac to dc converter can clear the ac side faster than the VCBs, if necessary.

All topologies with dc fault blocking capability have higher losses (more series semiconductors) than standard two level and MMC type converters (Chapter 17.3.4).

Reading list

General Electric Company, *Transient Voltage Suppression,* 400.3, 1982.

Grafham, D.R. *et al., SCR Manual,* General Electric Company, 6th Edition, 1979.

Fuse manufacturers

Eaton Electrical's Cutler-Hammer formerly Westinghouse, Ferraz Shawmut, S&C Electric, Efen, Siba, Edison, Brush, Bussmann, Littelfuse, Cooper Power Systems, General Electric, ABB, and Fusetek.

http://www.bussmann.co.uk/
http://www.sibafuses.com/
http://www.ferrazshawmut.com/

Problems

12.1 A three phase ac to dc thyristor bridge converter with one thyristor per leg has the following specification:

- 500 hp dc load machine - with nominal voltage: 660 V dc, maximum current: 600 A dc
- Supply transformer 750 kVA, 5% impedance
- Supply voltage - 480 V_{ac} rms.
- Overload protection is provided by a current limit circuit (direct control of thyristor firing) with a response time of 25 ms
- Maximum 40°C ambient, convection ventilation

Thyristor characteristics:

- I^2t 120,000 A^2s
- peak reverse voltage withstand (U_{rrm}) 1600 V

Specify a dc fuse when each thyristor is fuse protected. Assume a thyristor current utilisation factor of 58%. Estimate fuse losses.

(400A fuses, losses = 6x53W, 500A fuses, losses =6x34W)