CHAPTER 11

Device Series and Parallel Operation, Interference, and Grounding

This chapter considers various areas of power device application that are often overlooked, or at best, underestimated. Such areas include parallel and series device utilisation, radio frequency interference (rfi) noise, filtering, and interactive noise effects. The meaning of earth and neutral is explained.

The power-handling capabilities of power semiconductor devices are generally limited by device area utilisation, encapsulation, and cooling efficiency. Many high-power applications exist where a single device is inadequate and, in order to increase power capability, devices are paralleled to increase current capability or series-connected to increase voltage ratings. Extensive series connection of devices is utilised in HVDC transmission thyristor and IGBT modules while extensive paralleling of IGBTs is common in inverter applications. Devices are also series connected in multilevel converters.
When devices are connected in series for high-voltage operation, both steady-state and transient voltages must be shared equally by each individual series device. If power devices are connected in parallel to obtain higher current capability, the current sharing during both switching and conduction is achieved either by matching appropriate device electrical and thermal characteristics or by using external forced sharing techniques.

11.1 Series connection and operation of power semiconductor devices

11.1.1 Series semiconductor device operation

Owing to variations in blocking currents, junction capacitances, delay times, on-state voltage drops, and reverse recovery of individual power devices, external voltage equalisation networks and special gate circuits are required if devices are to be reliably connected and operated in series (or parallel).

11.1.1i - Steady-state voltage sharing

Figure 11.1 shows the forward off-state voltage-current characteristics of two power switching devices, such as SCRs or IGBTs. Both series devices conduct the same off-state leakage current but, as shown, each supports a different voltage. The total voltage blocked is $V_1 + V_2$ which can be significantly less than the sum of the individual voltage capabilities. Forced voltage sharing can be achieved by connecting a resistor of suitable resistance in parallel with each series device as shown in figure 11.2.

These equal value sharing resistors will consume power and it is therefore desirable to use as large resistance as possible. For worst case analysis consider n cells in series, where all the cells pass the maximum leakage current except cell D_1 which has the lowest leakage. Cell D_1 will support a larger blocking voltage than the remaining n - 1 which share voltage equally.
Let V_D be the maximum blocking voltage for any cell which in the worst-case analysis is supported by D_1. If the range of maximum rated leakage or blocking currents is from $\hat{I}_b$ to $\check{I}_b$ then the maximum imbalance occurs when member D_1 has a leakage current of $\check{I}_b$ whilst all the remainder conduct $\hat{I}_b$.

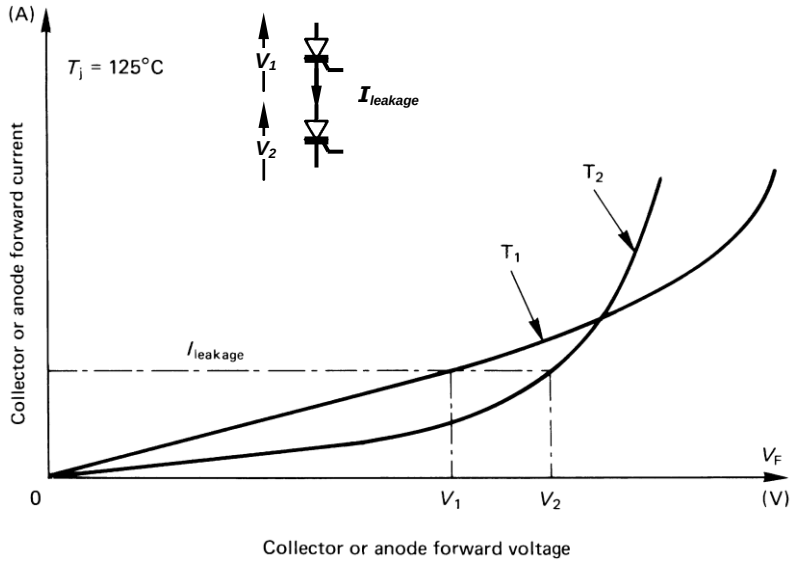


Figure 11.1. *Collector (transistor) or anode (thyristor) forward blocking I-V characteristics showing voltage sharing imbalance for two devices in series.*

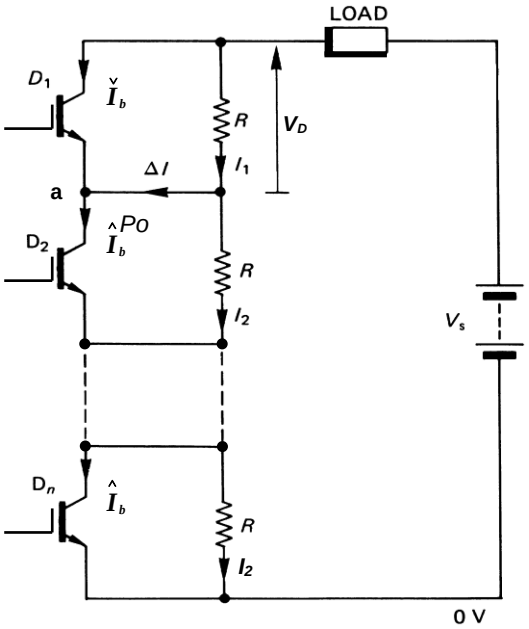


Figure 11.2. *Series IGBT string with resistive shunting for sustaining voltage equalisation in the off-state.*

From figure 11.2, Kirchhoff's current law at node 'a', gives

$$\Delta I = \hat{I}_b - \check{I}_b \quad \text{(A)} \tag{11.1}$$

$$= I_1 - I_2 \quad \text{(A)} \tag{11.2}$$

where $I_1 > I_2$. The voltage across cell D_1 is

$$V_D = I_1 R \quad \text{(V)} \tag{11.3}$$

By symmetry and Kirchhoff's voltage law, the total string voltage to be supported, V_s, is given by

$$V_s = (n - 1)\, I_2\, R + V_D \quad \text{(V)} \tag{11.4}$$

Eliminating ΔI, I_1, and I_2 from equations (11.1) to (11.4) yields

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\left(\hat{I}_b - \check{I}_b\right)} \quad (\text{ohms}) \tag{11.5}$$

for $n \ge 2$.

Generally only the maximum leakage current at rated voltage and maximum junction temperature is specified. By assuming $\check{I}_b = 0$, a conservative value of the maximum allowable resistance is obtained, namely

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\,\hat{I}_b} = \frac{n(1-k_s)V_D}{(n-1)\,\hat{I}_b} \underset{n\to\infty}{\approx} \frac{(1-k_s)V_D}{\hat{I}_b} \quad (\text{ohms}) \tag{11.6}$$

The extent to which nV_D is greater than V_s, is termed the *voltage sharing factor*, namely

$$k_s = V_s / nV_D \leq 1 \qquad (11.7)$$

As the number of devices is minimized the sharing factor approaches one, but equation (11.5) shows that undesirably the resistance for sharing decreases, hence losses increase.
The power dissipation of the resistor experiencing the highest voltage is given by

$$\hat{P}_d = V_D^2 / \hat{R} \quad \text{(W)} \qquad (11.8)$$

If resistors of ± l00a per cent resistance tolerance are used, the worst case occurs when cell D_1 has a parallel resistance at the upper tolerance while all the other devices have parallel resistance at the lower limit. After using $V_D = (1+a)I_1R$ and $V_s = (n-1)\times(1-a)\ I_2R + V_D$ for equations (11.3) and (11.4), the maximum resistance is given by

$$\hat{R} \leq \frac{n(1 - a)V_D - (1 + a)V_s}{(n - 1)(1 - a^2)\hat{I}_b} \quad \text{(ohms)} \qquad (11.9)$$

for $n \geq 2$.

The maximum loss in a resistor is

$$\hat{P}_D = V_D^2 / \hat{R}(1 - a) \qquad (11.10)$$

If the dc supply toleration is incorporated, then V_s in equations (11.6) and (11.9) is replaced by $(1+b)\times V_s$ where +100b is the supply percentage upper tolerance. This leads to a decreased resistance requirement, hence increased resistor power losses.

$$\hat{R} \leq \frac{n(1-a)V_D - (1+a)(1+b)V_s}{(n - 1)(1 - a^2)\hat{I}_b} \quad \text{(ohms)} \qquad (11.11)$$

The effects and importance of just a few per cent resistance or supply voltage tolerance on the maximum value for the sharing resistors and their power losses, are illustrated by example 11.1.

Example 11.1: ***Series device connection – static voltage balancing***

Ten, 200 V reverse-blocking, ultra fast 35 ns reverse recovery diodes are to be employed in series in a 1500 V dc peak, string voltage application. If the maximum device reverse leakage current is 10 mA (at maximum junction temperature) calculate the voltage sharing factor, and for worst-case conditions, the maximum value of sharing resistance and power dissipation.

i. If 10 per cent tolerance resistors are employed, what is the maximum sharing resistance and its associated power rating?
ii. If a further allowance for supply voltage tolerance of ±5% is incorporated, what is the maximum sharing resistance and its associated power rating?

Solution

When n = 10, V_D = 200 V dc, V_s = 1500 V dc, and $\hat{I}_b$ = 10mA, the voltage sharing factor is $k_s = 1500\text{V}/10\times200\text{V} = 0.75$. Equation (11.6) yields the maximum allowable sharing resistance

$$\hat{R} \leq \frac{nV_D - V_s}{(n-1)\hat{I}_b} = \frac{10\times200\text{V} - 1500\text{V}}{(10 - 1)\times10\text{mA}} = 5.55\text{k}\Omega$$

The nearest (lower) preferred value, 4.7kΩ, would be used.

Maximum resistor power losses occur when the diodes are continuously blocking. The maximum individual supporting voltage appears across the diode which conducts the least leakage current. Under worst-case conditions this diode therefore supports voltage V_D, hence maximum power loss $\hat{P}_D$ is

$$\hat{P}_D = V_D^2 / \hat{R}$$
$$= 200\text{V}^2/4700\Omega = 8.5\text{ W}$$

Since the worse device, (in terms of sharing has lowest leakage current), is randomly located in the string, each 4.7kΩ resistor must be capable of dissipating 8.5W.

The maximum 1500V dc supply leakage current is 42.5mA (10mA+1500V/10×4.7kΩ) giving 63.8W total losses (1500V×42.5mA), of which 15W (10mA×1500V) is lost in the diodes.

i. If 10% resistance tolerance is incorporated, equation (11.9) is employed with a **=** **+**0.1, that is

$$\hat{R} \le \frac{n(1 - a)V_D - (1 + a)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b}$$

$$\hat{R} \le \frac{10 \times (10 - 0.1) \times 200\text{V} - (1 + 0.1) \times 1500\text{V}}{(10 - 1) \times \left(1 - 0.1^2\right) \times 10\text{mA}}$$

$$= 2.13\ \text{k}\Omega$$

The nearest (lower) preferred value is 1.8kΩ, which is much lower resistance (higher losses) than if closely matched resistors were to be used.
Worst-case resistor power dissipation is

$$\hat{P}_D = V_D^2 / \hat{R}(1 - a)$$

$$= 200\text{V}^2/1800\Omega \times (1 - 0.1)$$

$$= 27.7\ \text{W}$$

The maximum total module losses are 165W (1500V×103mA) arising from 103mA (10mA + 1500V/1.8kΩ×(1- 0.1)) of leakage current.

ii. If the device with the lowest leakage is associated with the worst case resistance (upper tolerance band limit), and simultaneously the supply is at its upper tolerance limit, then worst case resistance is given by equation (11.11), that is

$$\hat{R} \le \frac{n(1-a)V_D - (1+a)(1+b)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b}$$

$$= \frac{10 \times (1 - 0.1) \times 200\text{V} - (1 + 0.1) \times (1 + 0.05) \times 1500\text{V}}{(10 - 1) \times \left(1 - 0.1^2\right) \times 10\text{mA}} = 758\Omega$$

Each resistor (preferred value 680Ω) needs to be rated in excess of

$$200\text{V}^2/680\Omega \times (1 - 0.1) = 68.6\ \text{W}$$

♣

When resistance tolerances are considered, sharing resistors of lower value must be used and the wider the tolerance, the lower will be the resistance and the higher the power losses. A number of solutions exist for reducing power losses and economic considerations dictate the acceptable trade-off level. Matched semiconductor devices would allow a minimum number of string devices (voltage sharing factor $k_s \rightarrow 1$) or, for a given string device number, a maximum value of sharing resistance (lowest losses). But matching is complicated by the fact that semiconductor leakage current varies significantly with temperature. Alternatively, by increasing the string device number (decreasing the sharing factor k_s) the sharing resistance is increased, thereby decreasing losses. By increasing the string device number from 10 (k_s = ¾) to 11 (k_s = 0.68) in example 11.1, the sharing resistance requirement increases from 4.7kΩ to 6.8kΩ and resistor losses are reduced from a total of 50.8 W to 31 W. Another method of minimising sharing resistance losses is to minimise resistance tolerances. A tolerance reduction from 10 per cent to 5 per cent in example 11.1 increases the sharing resistance requirements from 1.8kΩ to 3.9kΩ, while total power losses are reduced from 140 W to 64 W. These worst-case losses assume a near 100% off-state duty cycle.

11.1.1ii - Transient voltage sharing

During steady-state or at very low frequencies, sharing resistors as shown in figure 11.2 are sufficient to prevent individual device overvoltage. Mismatching of turn-on delay times of thyristors and transistors can be minimised by supplying high enough turn-on drive with fast rise times. A higher initial *di/dt* is then allowable.
Before a conducting string of diodes or thyristors can reverse-block, reverse recovery charge must flow. Those elements with least recovery charge requirements recover first and support the reverse bias. The un-recovered devices recover slowly, since recovery now occurs as a result of the low leakage current though the recovered devices, and natural recombination.
The transient reverse-blocking voltage can be shared more equally by placing capacitors across each string element as shown in figure 11.3. The capacitor action is to provide a transient current path bypassing a recovered device to allow a slower device to recover and to support volts. In the case of thyristors, low value resistance is connected in series with each capacitor to avoid high capacitor discharge through the thyristors at turn-on. Figure 11.4 shows the *I*-*V* characteristics of two unmatched thyristors or diodes during reverse recovery.

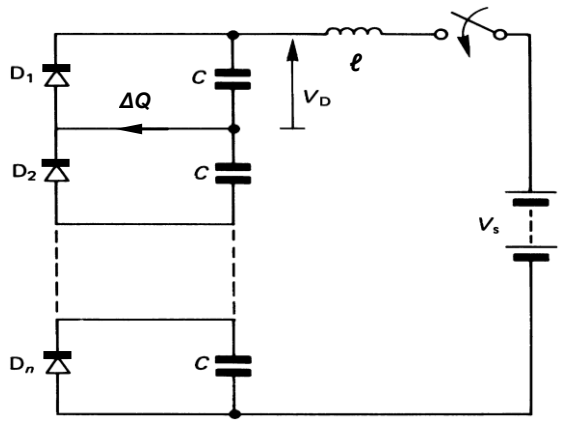


Figure 11.3. *A series diode string with shunting capacitance for transient reverse blocking voltage sharing.*

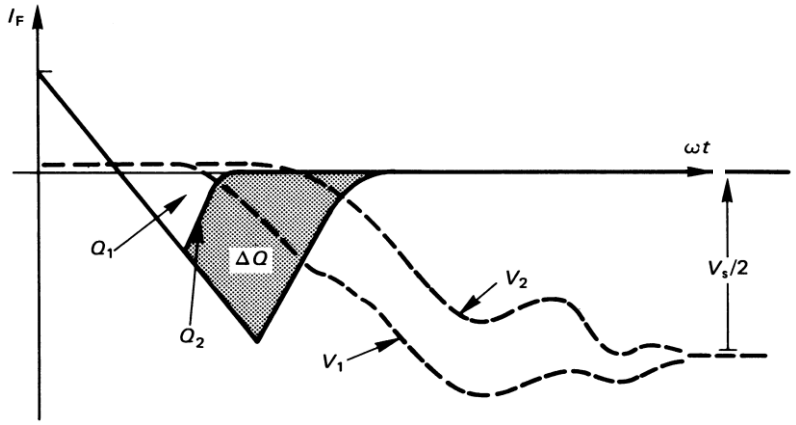


Figure 11.4. *Reverse recovery current and voltage for two mismatched series connected diodes.*

The worst case assumptions for the analysis of figure 11.3 are that element D_1 has minimum stored charge $\check{Q}$ while all other devices have the maximum requirement, $\hat{Q}$. The charge difference is

$$\Delta Q = \hat{Q} - \check{Q} \qquad \text{(C)} \qquad (11.12)$$

The total string dc voltage V_s, comprises the voltage across the fast-recovery device V_D plus the sum of each of the voltages across the slow n - 1 devices, V_{slow}. That is

$$V_s = V_D + (n - 1)V_{slow} \qquad \text{(V)} \qquad (11.13)$$

The voltage across each slow device is given by

$$V_{slow} = \frac{1}{n}\left(V_s - \Delta\hat{V}\right) \qquad \text{(V)} \qquad (11.14)$$

where $\Delta\hat{V} = \Delta\hat{Q}/C$.

Eliminating V_{slow} from equations (11.13) and (11.14) yields

$$\check{C} \geq \frac{(n-1)\,\Delta Q}{nV_D - V_s} = \frac{(n-1)\,\Delta Q}{n(1-k_s)V_D} \qquad \text{(F)} \qquad (11.15)$$

This equation shows that as the number of devices is minimized, the sharing factor, k_s, which is in the denominator of equation (11.15), tends to one and the capacitance requirement undesirably increases. Manufacturers do not specify the minimum reverse recovery charge but specify the maximum reverse recovery charge for a given initial forward current, reverse recovery *di/dt,* and temperature. For worst case design, assume $\check{Q}$ = 0, thus

$$\check{C} \geq \frac{(n-1)\hat{Q}}{nV_D - V_s} = \frac{(n-1)\hat{Q}}{n(1-k_s)V_D} \underset{n\to\infty}{\approx} \frac{\hat{Q}}{(1-k_s)V_D} \qquad \text{(F)} \qquad (11.16)$$

Voltage sharing circuit design is complicated if the effects of reverse steady-state leakage current in ac thyristor blocking are taken into account.

Supply and sharing capacitance tolerances significantly affect the minimum capacitance requirement. Worst case assumptions for capacitance tolerances involve the case when the fastest recovering diode is in parallel with capacitance at its lower tolerance limit while all the other sharing capacitances are at their upper tolerance limit. Assuming the minimum reverse recovery charge is zero, then the minimum sharing capacitance requirement is

$$\check{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - V_s)} = \frac{(n-1)\hat{Q}}{n(1-a)(1-k_s)V_D} \quad \text{(F)} \qquad (11.17)$$

where -100*a* is the capacitor negative percentage tolerance and $n \geq 2$. Voltage sharing resistors help minimise capacitor static voltage variation due to capacitance variations.

If the supply tolerance is incorporated, then V_S in equations (11.16) and (11.17) are replaced by $(1+b)\times V_S$ where +100*b* is the supply percentage upper tolerance. This leads to an increased capacitance requirement, hence increased energy losses, $\frac{1}{2}C V_D^2$.

$$\check{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - (1+b)V_s)} \quad \text{(F)} \qquad (11.18)$$

Example 11.2: ***Series device connection – dynamic voltage balancing***

The string of ten, 200 V diodes in worked example 11.1 is to incorporate capacitive reverse recovery transient sharing. Using the data in chapter 5, figure 5.9, specify a suitable sharing capacitance based on zero capacitance and supply tolerances ($a = b = 0$), then ± 10 per cent capacitance tolerances ($a = 0.1$, $b = 0$), ± 5 per cent supply tolerance ($a = 0$, $b = 0.05$), then both tolerances ($a = 0.1$, $b = 0.05$). Estimate in each case the capacitor energy loss at capacitor discharge.

Solution

Figure 5.9 shows that worst-case reverse recovery conditions occur at maximum junction temperature, *di/dt,* and I_F, and a value of $\hat{Q} = 6\mu C$ is appropriate.
The minimum possible sharing capacitance occurs when the capacitance and dc rail voltage are tightly specified. From equation (11.16)

$$\check{C} \geq \frac{(n-1)\hat{Q}}{nV_D - V_s} = \frac{(10\text{-}1)\times 6\mu C}{10\times 200V - 1500V} = 108nF \text{ @ } 200Vdc$$

The sharing capacitance requirement with 10% tolerance capacitors, is given by equation (11.17)

$$\check{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - V_s)} = \frac{(10 - 1)\times 6\mu C}{(1 - 0.1)\times(10\times 200V\text{-}1500V)} = 0.12\mu F \text{ @ } 200Vdc$$

A further increase in capacitance requirement results if the upper tolerance dc rail voltage is used. From equation (11.18)

$$\check{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - (1+b)V_s)}$$

$$= \frac{(10 - 1)\times 6\mu C}{(1 - 0.1)\times(10\times 200V - (1+0.05)\times 1500V)} = 0.14\mu F \text{ @ } 200Vdc$$

In each tolerance case the next larger preferred capacitance value should be used, namely, 120nF, 120nF, and 150nF respectively, all rated at 200V dc.
The total series capacitance, using the upper tolerance limit is

$$C_T = \frac{(1+a)\check{C}}{n}$$

The stored energy with a 1500V dc rail in the 10 series connect 120nF capacitors, and subsequently loss when the string voltages reduces to zero at diode forward bias, is therefore

$$W_T = \tfrac{1}{2}C_T\hat{V}_s^2 = \tfrac{1}{2}\frac{(1+a)\check{C}}{n}V_s^2(1+b)^2$$

$$= \tfrac{1}{2}\frac{(1 + 0.1)\times 120nF}{10}\times 1500V^2\times(1+0.05)^2 = 16.4mJ$$

The energy stored in the 10 series connect 150nF capacitors, and subsequently loss when the string voltage reduces to zero at diode forward bias, is

$$W_T = \tfrac{1}{2}\times\frac{(1 + 0.1)\times 150nF}{10}\times 1500V^2\times(1 + 0.05)^2 = 20.5mJ$$

♣

When capacitive sharing is used with switching devices, at turn-on the transient sharing capacitor discharges into the switching device. The discharge current magnitude is controlled by the turn-on voltage fall characteristics. If a linear voltage fall at turn-on is assumed, then the transient sharing capacitor maximum discharge current i_{dis} is a constant current pulse for the fall duration, of magnitude

$$i_{dis} = C\frac{\Delta V_D}{\Delta t} = C\frac{V_D}{t_{tv}} \quad \text{(A)} \qquad (11.19)$$

The discharge current can be of the order of hundreds of amperes, incurring initial *di/dt* values beyond the capabilities of the switching device. In example 11.2 the discharge current for a switch rather than a diode is approximately 150nF×200V/1μs =30A, assuming a 1μs voltage fall time. This 30A may not be insignificant compared to the switches current rating. But, advantageously, the sharing capacitors do act as turn-off snubbers, reducing switch turn-off stressing.
In the case of the thyristor, the addition of a low-valued, low inductance, resistor in series with each transient capacitor can control the capacitor discharge current, yet not significantly affect the transient sharing properties. The resultant *R-C* discharge current can provide thyristor latching current while still offering transient recovery sharing, *dv/dt,* and voltage spike suppression. Thyristor snubber operation and design are considered in chapter 9.1.2.

Figure 11.5 shows the complete steady-state and transient-sharing networks used for diodes, thyristors, and transistors. Transient voltage sharing for transistors involves the use of the conventional *R-D-C* snubber shown in figure 11.5c and considered in chapter 9. The series inductor used with thyristor and transistor strings provides transient turn-on voltage protection. The inductor supports the main voltage while each individual element switches on. Such an inductive turn-on snubber is mandatory for the GCT and the GTO thyristor. No one device is voltage-stressed as a consequence of having a longer turn-on delay time, although gate overdrive at turn-on minimises delay variations.

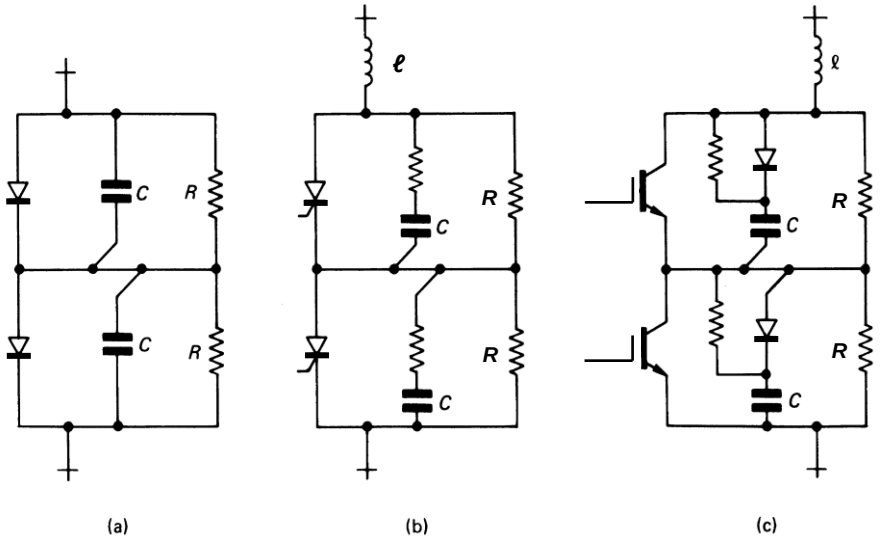


Figure 11.5. *Transient and steady-state voltage sharing circuits for series connected: (a) diodes; (b) thyristors; and (c) igbt transistors.*

11.2 Parallel connection and operation of power semiconductor devices

11.2.1 Parallel semiconductor device operation

It is common practice to parallel power devices in order to achieve higher current ratings or lower conducting voltages than are attainable with a single device. Although devices in parallel complicate layout and interconnections, better cooling distribution is obtained. Also, built-in redundancy can give improved equipment reliability. A cost saving may arise with extensive parallel connection of smaller, cheaper, high production volume devices.

The main design consideration for parallel device operation is that all devices share both the steady-state and transient currents. Any bipolar device carrying a disproportionately high current will heat up and conduct more current, eventually leading to thermal runaway as considered in section 4.1.
The problem of current sharing is less severe with diodes because diode characteristics are more uniform (because of their simpler structure and manufacturing) than those of thyristors and transistors.

Two basic sharing solutions exist

- matched devices
- external forced current sharing.

11.2.1i - Matched devices

Figure 11.6 shows the static I-V on-state characteristics of two SCR's. If these two devices are connected in parallel, for the same on-state voltage, the resultant current flow is $I_1 + I_2$ where I_1 and I_2 can be very different in value. The total current rating of the pair is not the sum of the maximum current rating for each but rather a value which can be just larger than the rating of one device alone. The percentage parallel derating *pd* for *n* parallel connected devices is defined as

$$pd = \left(1 - \frac{I_T}{nI_m}\right) \times 100 \quad = \left(1 - k_p\right) \times 100 \quad \text{per cent} \tag{11.20}$$

where I_T = total current through the parallel arrangement
I_m = maximum allowable single device current rating
n = number of parallel devices
k_p = current parallel sharing factor = $I_T/nI_m \leq 1$

Parallel connection of IGBT die within a module is made possible by using die from the same wafer/batch. On-state voltage matching for single large area wafers is expensive and complicated by the high temperature dependence of both static and dynamic electrical device characteristics.
Derating does not account for effects such as layout and electrical and thermal impedance imbalance. The amount of derating is traded off against the extra cost involved in selecting devices with closer (matched) static characteristics.

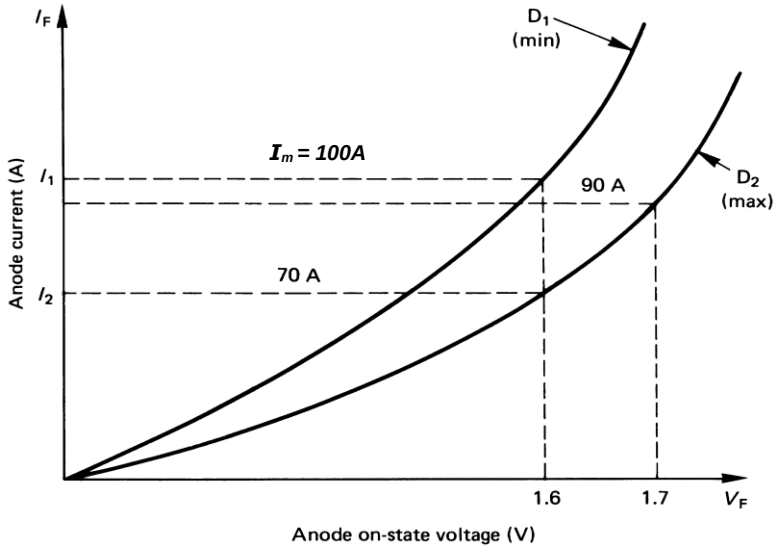


Figure 11.6. *Forward conduction characteristics of two unmatched devices.*

11.2.1ii - External forced current sharing

Forced current sharing is applicable to both steady-state and transient conditions. For a current derating of less than 5 per cent it is usually cheaper to use forced sharing techniques rather than matched devices.
Figure 11.6 shows the maximum variation of I-V characteristics in devices of the same type. When parallel connected the maximum current is restricted to I_m+I_2, (= 100A+70A = 170A at 1.6V). The maximum current rating for each device is I_m, (100A); hence with suitable forced sharing a combination in excess of $I_m + I_2$ (170A) should be possible. The resistive network in figure 11.7 is used for forced current sharing and in example 11.3 it is required that I_m, 100A, flows through D_1 and (1-2×*pd*)× $I_m > I_2$, (90A) flows through D_2, for a *pd* (5%) overall derating.

From Kirchhoff's voltage law in figure 11.7

$$\begin{aligned} V_1 + V_3 &= V_2 + V_4 \\ V_{D_1} + I_m R &= V_{D_2} + \left(I_T - I_m\right) R \end{aligned} \tag{11.21}$$

From equation (11.20), rearranged for two devices, n = 2

$$I_T = 2 \times (1 - pd) I_m = 2 k_p I_m$$

Substituting for I_T in equation (11.21) gives

$$R = \frac{V_{D_2} - V_{D_1}}{2\ pd\ I_m} \quad \text{(ohms)} \tag{11.22}$$

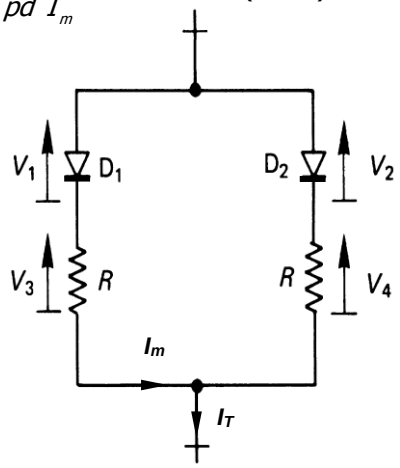


Figure 11.7. *Forced current sharing network for parallel connected devices.*

For *n* devices connected in parallel, equation (11.21) becomes

$$V_{D_1} + I_m R = V_{D_2} + \frac{(I_T - I_m)}{n-1} R \tag{11.23}$$

which after substituting for I_T from equation (11.20), for maximum device voltage variation, gives

$$R = \frac{\hat{V}_D - \check{V}_D}{I_m} \frac{(n-1)}{n \times pd} \quad \text{(ohms)} \tag{11.24}$$

Although steady-state sharing is effective, sharing resistor losses can be high. The total resistor losses in general terms for *n* parallel connected devices and a conduction duty cycle δ, are given by

$$P_t = \delta \left\{ 1 + \left(1 - \frac{n}{n-1} \times pd \right)^2 \right\} I_m^2 R \quad \text{(W)} \tag{11.25}$$

Since the devices are random in characteristics, each resistor must have a power rating of $I_m^2 R$.

Example 11.3: ***Resistive parallel current sharing – static current balancing***

For the two diodes shown in figure 11.6, with $\hat{I} = 100\text{A}$, what derating results when they are parallel connected, without any external sharing circuits?
The maximum current rating for each device is I_m, 100A; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 11.7 for current sharing, it is required that 100A flows through D_1 and 90A through D_2. Specify the per cent overall derating, the necessary sharing resistors, their worst case losses and diode average, rms, and ac currents at a 50% duty cycle and worst case.

Solution

The derating for the parallel situation depicted in figure 11.6, without external sharing, is

$$pd = \left(1 - \frac{170\text{A}}{2 \times 100\text{A}} \right) \times 100 = 15 \text{ per cent} \qquad \left(k_p = \frac{100\text{A} + 70\text{A}}{2 \times 100\text{A}} = 0.85 \right)$$

With forced resistive sharing, the objective derating is reduced from 15% to

$$pd = \left(1 - \frac{190\text{A}}{2 \times 100\text{A}} \right) \times 100 = 5 \text{ per cent} \qquad \left(k_p = \frac{100\text{A} + 90\text{A}}{2 \times 100\text{A}} = 0.95 \right)$$

From figure 11.6

$$1.6\text{V} + 100\text{A} \times \text{R} = 1.7\text{V} + 90\text{A} \times \text{R}$$

that is

$$R = 10 \text{ milliohm}$$

Equation (11.22), being based on the same procedure, gives the same result. The cell voltage drop is increased to $1.6\text{V} + 100\text{A} \times 0.01\Omega = 1.7\text{V} + 90\text{A} \times 0.01\Omega = 2.6\text{V}$.

Thus, for an on-state duty cycle δ, the total losses are δ×2.6V×190A = δ×494W.
For $\delta = ½$

$$\bar{I}_{D1} = \delta \times I_{D1} = ½ \times 100\text{A} = 50\text{A} \qquad \bar{I}_{D2} = \delta \times I_{D2} = ½ \times 90\text{A} = 45\text{A}$$

$$I_{D1rms} = \sqrt{\delta} \times I_{D1} = \sqrt{½} \times 100\text{A} = 70.7\text{A} \qquad \bar{I}_{D2rms} = \sqrt{\delta} \times I_{D2} = \sqrt{½} \times 90\text{A} = 63.6\text{A}$$

$$I_{D1ac} = \sqrt{I_{D1rms}^2 - \bar{I}_{D1}^2} = \sqrt{70.7^2 - 50^2} = 50\text{A} \qquad I_{D2ac} = \sqrt{I_{D2rms}^2 - \bar{I}_{D2}^2} = \sqrt{63.6^2 - 45^2} = 45\text{A}$$

$$P_{R1} = I_{D1rms}^2 R_1 = 70.7^2 \times 0.01\text{m}\Omega = 50\text{W} \qquad P_{R2} = I_{D2rms}^2 R_2 = 63.6^2 \times 0.01\text{m}\Omega = 40.5\text{W}$$

$$P_{D1} = \bar{I}_{D1} V_{D1} = 50\text{A} \times 1.6\text{V} = 80\text{W} \qquad P_{R2} = \bar{I}_{D2} V_{D2} = 45\text{A} \times 1.7\text{V} = 76.5\text{W}$$

$$P_{total} = P_R + P_D = (50\text{W} + 40.5\text{W}) + (80\text{W} + 76.5\text{W}) = 90.5\text{W} + 156.5\text{W} = 247\text{W}$$

For worst case losses, $\delta \to 1$

$$\bar{I}_{D1} = \delta \times I_{D1} = 1 \times 100\text{A} = 100\text{A} \qquad \bar{I}_{D2} = \delta \times I_{D2} = 1 \times 90\text{A} = 90\text{A}$$

$$I_{D1rms} = \sqrt{\delta} \times I_{D1} = \sqrt{1} \times 100\text{A} = 100\text{A} \qquad \bar{I}_{D2rms} = \sqrt{\delta} \times I_{D2} = \sqrt{1} \times 90\text{A} = 90\text{A}$$

$$I_{D1ac} = \sqrt{I_{D1rms}^2 - \bar{I}_{D1}^2} = \sqrt{100^2 - 100^2} = 0\text{A} \qquad I_{D2ac} = \sqrt{I_{D2rms}^2 - \bar{I}_{D2}^2} = \sqrt{90^2 - 90^2} = 0\text{A}$$

$$P_{R1} = I_{D1rms}^2 R_1 = 100^2 \times 0.01\text{m}\Omega = 100\text{W} \qquad P_{R2} = I_{D2rms}^2 R_2 = 90^2 \times 0.01\text{m}\Omega = 81\text{W}$$

$$P_{D1} = \bar{I}_{D1} V_{D1} = 100\text{A} \times 1.6\text{V} = 160\text{W} \qquad P_{R2} = \bar{I}_{D2} V_{D2} = 90\text{A} \times 1.7\text{V} = 153\text{W}$$

$$P_{total} = P_R + P_D = (100\text{W} + 81\text{W}) + (160\text{W} + 153\text{W}) = 181\text{W} + 313\text{W} = 494\text{W}$$

The general form in equation (11.25) gives the same total resistor losses for each conduction duty cycle case, namely for $\delta = ½$: 50W+40.5W = 90.5W and for $\delta \to 1$: 100W+81W = 181W.

♣

A more efficient method of current sharing is to use coupled reactors as shown in figure 11.8. In these feedback arrangements, in figure 11.8a, if the current in D_1 tends to increase above that through D_2, the voltage across L_1 increases to oppose current flow through D_1. Simultaneously a negative voltage is induced across L_2 thereby increasing the voltage across D_2 thus increasing its current. This technique is most effective in ac circuits where the core is more readily designed to reset, avoiding saturation.

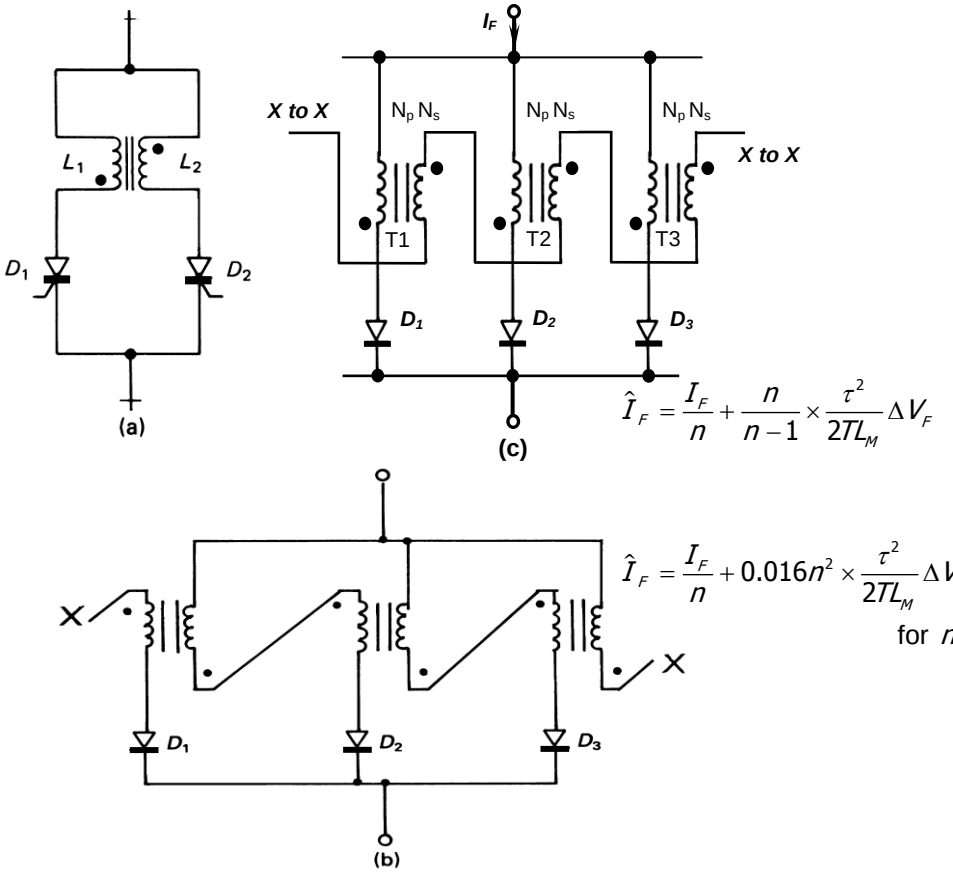


Figure 11.8. *External forced current sharing networks using cross-coupled reactors: (a) for two devices; and (b) and (c) for many devices.*

Equalising reactor arrangements are possible for any number of devices in parallel, as shown in figures 11.8b and c, but size and cost become limiting constraints. The technique is applicable to steady-state and transient sharing. At high current densities, the forward *I-V* characteristics of diodes and thyristors (and some IGBTs) have a positive temperature dependence which provides feedback aiding sharing.
The mean current in the device with the highest current, therefore lowest voltage, of *n* parallel connected devices in figure 11.8c (with one coupled circuit in series with each device), is given by

$$\bar{I}_F = \frac{I_F}{n} + \Delta I_F = \frac{I_F}{n} + \frac{n-1}{n} \times \frac{\tau^2}{2TL_M} \Delta V_F = \frac{I_F}{n} + \frac{n-1}{n} \times \frac{\delta^2}{2f_s L_M} \Delta V_F \qquad (11.26)$$

where ΔV_F is the maximum on-state voltage drop difference
L_M is the self-inductance (magnetising inductance) of the coupled inductor
T is the cycle period, $1/f_s$, and
τ is the conduction period ($\tau < T$)

(a) current sharing analysis for two devices:– $r_o = 0$
Consider two thyristors (n = 2) connected in parallel as show in figure 11.9. The coupled circuit magnetising current is modelled with the magnetising inductor L_M. The transformer turns ratio is 1:1, hence the winding voltages and currents are equal, taking into account the relative winding flux orientation shown by the dots. Commutation inductance overlap is ignored.
From Kirchhoff's voltage law

$$v_{T1} + v_1 = v_{T2} - v_1 \qquad (11.27)$$

That is

$$v_1 = ½ \times (v_{T1} - v_{T2}) = ½ \times \Delta v \qquad (11.28)$$

From Kirchhoff's current law

$$I_M = i_1 - i_2 \qquad (11.29)$$

From Faraday's equation

$$v_1 = L_M \frac{dI_M}{dt} \qquad (11.30)$$

which after integrating both sides gives

$$I_M = \frac{1}{L_M} \int_0^{\tau} v_1 dt = ½ \frac{1}{L_M} \Delta V_F \tau \qquad (11.31)$$

As a condition it is assumed that the voltage difference Δv does not decrease as the operating point moves along the *I-V* characteristics. That is, both devices are modelled by $v = v_o + i \times r_o$, where the linear resistance r_o, is zero, each have different zero current voltages that is different v_o, $\Delta v_o = \Delta V_F$. Actually D_1 moves further up the *I-V* characteristic with time as it conducts more current while D_2 moves towards the origin, as shown in figure 11.9b.

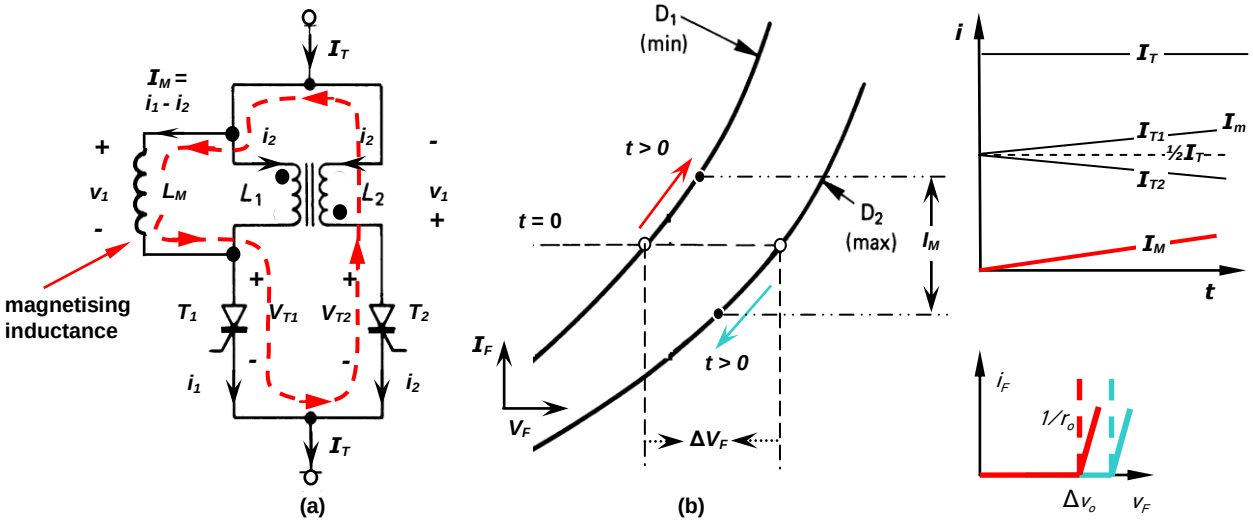


Figure 11.9. *External forced current sharing network using cross-coupled reactors: (a) circuit (including magnetising inductance L_M) for two devices and (b) I-V operating points.*

(b) current sharing analysis for two devices:– $r_o \neq 0$
If static resistance is included in the device model for current sharing analysis, then equation (11.30), assuming both devices have the equal resistance, becomes

$$\Delta v_o = L_M \frac{dI_M}{dt} + 2I_M r_o \qquad (11.32)$$

The solution to this differential equation gives the magnetizing current as

$$I_M = \frac{\Delta v_o}{2r_o}\left[1 - e^{-t\frac{2r_o}{L_M}}\right] \tag{11.33}$$

The maximum magnetizing current increases from zero and reaches a maximum at the end of the current conduction period τ. Re-arranging equation (11.33) gives the magnetizing inductance as

$$L_M = \frac{2r_o\tau}{\ell \mathrm{n}\left(\frac{\Delta v_o}{\Delta v_o - I_M 2r_o}\right)} \tag{11.34}$$

(c) current sharing analysis for *n* devices:– $r_o = 0$

When more than two devices are parallel connected, sharing can be enforced with the multiple transformer technique shown in figure 11.8c, where the ***n*** transformer secondary windings are series connected. Each transformer has a turns ratio of $\eta = N_p{:}N_s$, and the magnetising inductance is assumed to be on the primary side of each transformer.

The semiconductor devices are assumed to have a constant on-state voltage v_o. The total current is I_T, and zero commutation inductance is assumed.

Using Kirchhoff's voltage law on the primary side:

Since the secondary voltages sum to zero

$$v_{s1} + v_{s2} + v_{s3} + \ldots + v_{sn} = 0 \tag{11.35}$$

then the transformer primary voltages also sum to zero

$$v_{p1} + v_{p2} + v_{p3} + \ldots + v_{pn} = \frac{N_s}{N_p}\left(v_{s1} + v_{s2} + v_{s3} + \ldots + v_{sn}\right) = 0 \tag{11.36}$$

Since the legs are parallel connected

$$V_{T1} + v_{p1} = V_{T2} + v_{p2} = \ldots\ldots = V_{Tn} + v_{pn} \tag{11.37}$$

For worst case analysis, let one device ($n = 1$) operate at minimum on-state voltage, $\check{V}_T$, while the other $n - 1$ devices have a maximum on-state voltage $\hat{V}_T$, therefore potentially conduct less current than the device operating at minimum voltage.

$$\check{V}_T + v_{p1} = \hat{V}_T + v_p = \ldots\ldots = \hat{V}_T + v_p \tag{11.38}$$

These equations yield the following primary voltages

$$v_{p1} = \frac{n-1}{n}\left(\hat{V}_T - \check{V}_T\right) \quad \text{and} \quad v_{p2} = v_{p3} \ldots = v_{pn} = -\frac{1}{n}\left(\hat{V}_T - \check{V}_T\right) \tag{11.39}$$

Using Kirchhoff's current law on the primary side:

$$I_T = I_{T1} + I_{T2} + \ldots + I_{TN} \tag{11.40}$$

But a thyristor current, which is the transformer primary current, can be expressed in terms of the transformer secondary current plus the parallel magnetising current on the primary side. That is

$$I_{Ti} = i_{pi} + i_{Mi} = \frac{N_s}{N_p} i_s + i_{Mi} = \frac{1}{\eta} i_s + i_{Mi} \tag{11.41}$$

where, because the secondary windings are series connected, the secondary current is the same for each transformer. The transformer magnetising current i_{Mi} is the same for transformers $i = 2$ to n, i_M. Thus the total current

$$\begin{aligned} I_T &= \sum_{i=1}^{n} I_{Ti} = \sum_{i=1}^{n}\left(\frac{1}{\eta} i_s + i_{Mi}\right) \\ I_T &= n\frac{1}{\eta} i_s + i_{M1} + (n-1) i_M \end{aligned} \tag{11.42}$$

Using Kirchhoff's voltage law on the secondary side:

Since the transformers are identical, each has the same value of magnetising inductance (self-inductance) L_M. Because the secondary windings are series connected the sum of the secondary voltages, hence sum of primary voltages, are zero.

$$\begin{aligned} v_{p1} + v_{p2} + v_{p3} + \ldots + v_{pn} &= 0 \\ = L_M \frac{d\,i_{M1}}{dt} + L_M \frac{d\,i_{M2}}{dt} + \ldots\ldots + L_M \frac{d\,i_{Mn}}{dt} &= 0 \\ = L_M \left(\frac{d\,i_{M1}}{dt} + (n-1)\frac{d\,i_M}{dt} \right) &= 0 \\ = L_M \frac{d}{dt}\left[i_{M1} + (n-1) i_M \right] &= 0 \end{aligned} \tag{11.43}$$

The component inside the square bracket must be a constant.

$$i_{M1} + (n-1) i_M = \mathrm{c} \tag{11.44}$$

Substituting the constant c into equation (11.42) gives the secondary current as

$$i_s = \eta \frac{1}{n}(I_T - \mathrm{c}) \tag{11.45}$$

In conjunction with Faraday's equation, the magnetising current is a linear function of time, starting from zero. Applying these conditions to the worst case device, T1, then as the magnetising current in transformer Tr1 increases and the associated thyristor current I_{T1} increases, from equation (11.44), the opposing magnetising current in the other transformers reduces the associated device principal current. At the maximum on-time, the current in device T1 should not exceed its permitted rated limit, I_m.

$$\Delta i_{M1}(t) = \frac{1}{L_M} \times v_{p1} t \tag{11.46}$$

From equation (11.39), when $t = \tau$, the maximum magnetising current, in terms of the device voltage extremes, is

$$\Delta i_{M1}(t = \tau) = \Delta \hat{i}_{M1} = \frac{1}{L_M} \times \frac{n-1}{n} \left(\hat{V}_T - \check{V}_T \right) \times \tau \tag{11.47}$$

Re-arranging gives the necessary minimum transformer self-inductance with respect to the primary side.

$$L_M = \frac{1}{\Delta \hat{i}_{M1}} \times \frac{n-1}{n} \left(\hat{V}_T - \check{V}_T \right) \times \tau = \frac{1}{\Delta \hat{i}_{M1}} \times \frac{n-1}{n} \times \Delta V_F \times \tau \tag{11.48}$$

The maximum magnetising current $\Delta \hat{i}_{M1}$ can be expressed in terms of devices current rating I_m and device percentage derating, *pd,* or device utilisation, $k_p = 1 - pd$.

If the device current rating is I_m, then *n* devices in parallel can theoretically conduct $n \times I_m$. When derated by *pd* to k_p, the total current is $k_p \times n I_m$ where each device initially conducts $k_p \times I_m$. The current in the worst-case device increases from $k_p I_m$ to I_m ($\Delta \hat{i}_{M1} = (1 - k_p) I_m = pd \times I_m$) in the maximum period the device conducts, τ.

$$\hat{I}_T = k_p I_m + \Delta \hat{i}_M = k_p I_m + (1 - k_p) I_m = I_m \tag{11.49}$$

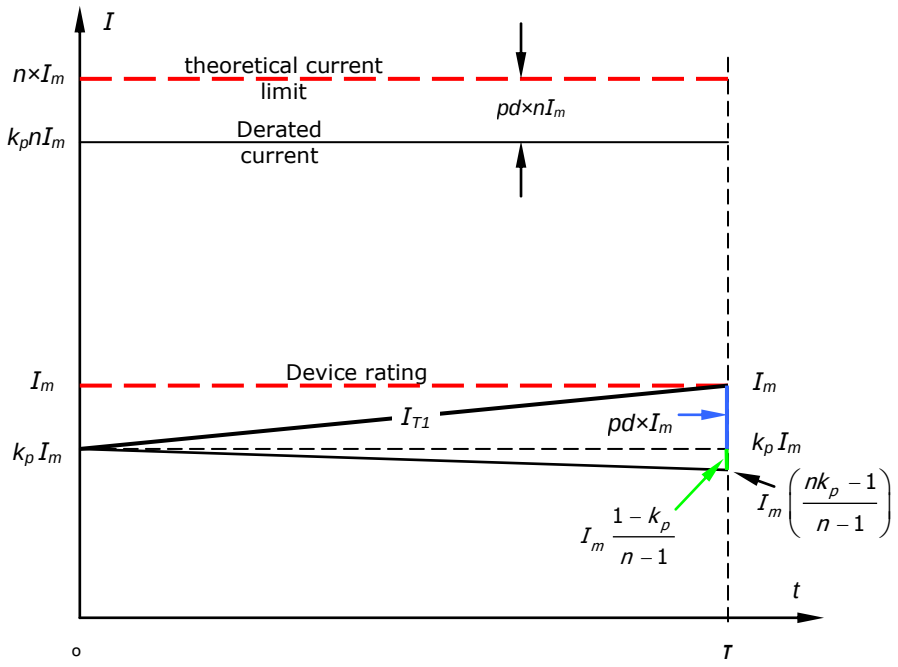


Figure 11.10. *External forced current sharing network using series connected secondary windings.*

The current in each of the remaining n-1 devices decreases from $k_p I_m$ by (1-k_p) I_m/n-1 to

$$\check{I}_T = k_p I_m - I_m \frac{1-k_p}{n-1} = I_m \left(\frac{nk_p - 1}{n-1} \right) \qquad (11.50)$$

such that the necessary total current is maintained:

$$\hat{I}_T + (n-1)\check{I}_T = I_m + (n-1) I_m \left(\frac{nk_p - 1}{n-1} \right) = nk_p I_m$$

These various current components are shown in figure 11.10.
By assuming a current quadratic dependence on time, equations similar to equations (11.26) can be obtained.

Example 11.4: ***Transformer current sharing – static and dynamic current balancing***

Two thyristors with the same forward conduction characteristics as the diodes in figure 11.6 are parallel connected using the coupled circuit arrangement in figure 11.8a.
The maximum current rating for each device is I_m, 100A; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 11.9a for current sharing, it is required that no more than rated current flow through the lower conducting voltage device, D_1. Specify the per cent overall derating and the necessary sharing transformer properties assuming a half-wave, 180º conduction, phase-controlled, 50Hz, highly inductive load application.
What are the transformer core reset requirements?
Estimate inductance requirements if the thyristors have a static on-state resistance of 1mΩ.

Solution

As in example 11.3, the derating for the parallel situation depicted in figure 11.6, without external sharing, is

$$pd = \left(1 - \frac{170\text{A}}{2\times 100\text{A}} \right) \times 100 = 15 \text{ per cent} \quad (k_p = 0.85)$$

With forced transformer sharing, the objective derating is reduced from 15% to

$$pd = \left(1 - \frac{190\text{A}}{2\times 100\text{A}} \right) \times 100 = 5 \text{ per cent} \quad (k_p = 0.95)$$

When the two thyristors are turned on, the magnetizing current is assumed zero and transformer action will force each device to conduct 95A, giving 190A in total. From figure 11.6, the voltage difference between the thyristors, ΔV_F is about 0.1V, thus the transformer winding voltages will be 0.05V each, with polarities as shown in figure 11.9a. In time the magnetizing current increases and the current in T**1** increases above 95A due to the increasing magnetizing current, while the current in T**2** decreases below 95A, such that the total load current is maintained at 190A.

The worst case conduction period in this ac application, giving maximum magnetising current, is for 180º conduction, that is, 10ms. Thus it is required that T**1** current rises to 100A and T**2** current falls to 90A at τ =10ms, that is, the magnetising current is 100A - 90A = 10A.
Substitution into equation (11.31) gives

$$L_M = ½ \frac{1}{I_M} \int_0^{10\text{ms}} \Delta v \, dt = ½ \times \frac{1}{10\text{A}} \times 0.1\text{V} \times 10\text{ms} = 50\mu\text{H}$$

where it is assuming that the voltage differential ΔV_F between the two devices is constant during the conduction period. In fact figure 11.9b shows that the voltage difference decreases, so assuming a constant value gives an under-estimate of requirements.

The core volt-µs during conduction is 0.05V×10ms = 500 V-µs. That is, during core reset the reverse voltage time integral must be at least 500 V-µs to ensure the core flux is reset, (magnetising current reduced to zero).
Using equation (11.34), with r_o = 1mΩ, gives

$$L_M = \frac{2 r_o \tau}{\ell \text{n} \left(\frac{\Delta v_o}{\Delta v_o - I_M 2 r_o} \right)} = \frac{2 \times 1\text{m}\Omega \times 10\text{ms}}{\ell \text{n} \left(\frac{0.1\text{V}}{0.1\text{V} - 10\text{A} \times 2 \times 1\text{m}\Omega} \right)} = 90\mu\text{H}$$

The inductance, 50µH, given by equation (11.31) when neglecting model resistance, under-estimates requirements.

♣

11.3 Interference

Electromagnetic phenomenon, whether intentional or unintentional by-products, tend to result in undesirable consequences in power electronic circuits and equipment, in terms of generated noise and susceptibility.

- EMC - *Electromagnetic Compatibility*
  The ability of a component or its associated system to operate and function correctly in its intended electromagnetic environment.

- EMI - *Electromagnetic Interference*
  Electromagnetic emissions from a component or its associated system that interfere with the normal operation of another component or system, or the emitting component or system itself.

11.3.1 Noise

RFI noise (electromagnetic interference, EMI) and the resultant equipment interaction is an area of power electronic design that is often fraught, under-estimated or overlooked.
EMI is due to the effects of undesired energy transfer caused by radiated electromagnetic fields or conducted voltages and currents. The interference is produced by a source emitter and is detected by a susceptible victim via a coupling path. The source itself may be a self-inflicted victim. The effects of this interference can vary from simple intermittent reset conditions to a catastrophic failure.

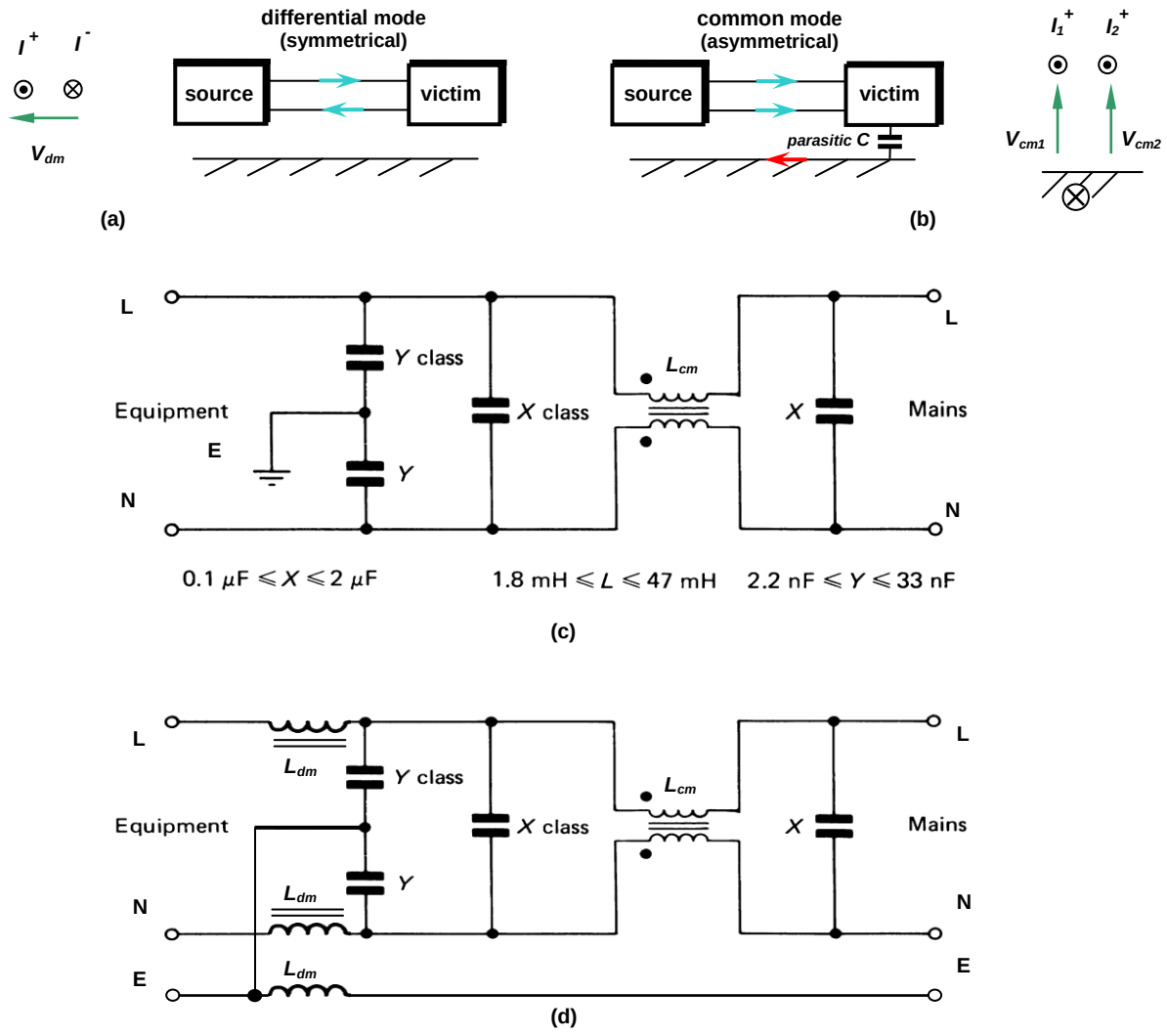


Figure 11.11. *Common mode & differential mode mains supply noise filtering: (a) differential mode noise paths; (b) common mode noise paths; (c) simple L-C mains filter; and (d) high specification mains filter.*

The coupling path may involve one or more of the following four coupling mechanisms.

- *Conduction* - electric current, I
- *Radiation* - electromagnetic field, Z_o
- *Capacitive coupling* - electric field, E
- *Inductive coupling* - magnetic field, H

11.3.1i - Conducted noise is coupled between components through interconnecting wiring such as through power supply (both ac and dc supplies) and ground wiring and planes. This common impedance coupling is caused when currents from two or more circuits flow through the same wiring impedance. Coupling can also result because of common mode and differential (symmetrical) currents, which are illustrated in figure 11.11. Two forms of common mode currents exist. When the conducting currents are equal such that $V_{cm1} = V_{cm2}$, then the common mode currents are termed asymmetrical, while if $V_{cm1} \neq V_{cm2}$, then the currents are termed non-symmetrical.

11.3.1ii - Radiated electromagnetic field coupling can be considered as two cases, namely

- near field, $r << \lambda / 2\pi$, where radiation due to electric fields, E, and magnetic fields, H, are considered separate
- far field, $r >> \lambda / 2\pi$, where the coupling is treated as a plane wave.

The boundary between the near and far field is given by $r = \lambda / 2\pi$ where λ is the noise wavelength and r is distance from the source.
As a reference impedance, the characteristic impedance of free space in the far field Z_o, is given by E / H, which is constant, $\sqrt{\mu_o / \varepsilon_o} = 120\pi = 377\Omega$.

In the ***near field*** region, the equation r^{-3} (as opposed to r^{-2} and r^{-1}) term dominates field strength.

- A wire currying current produces E α r^{-3} and H α r^{-2}, (common mode radiation)
  - thus the electric field E dominates and the wave impedance $Z > Z_o$.
- A wire loop carrying current produces H α r^{-3} and E α r^{-2}, (differential mode radiation)
  - thus the magnetic field H dominates and the wave impedance $Z < Z_o$.

In the near field, interference is dominated by the effective input impedance, Z_{in}, of the susceptible equipment and the source impedance R_s of its input drive.

- electric coupling increases with increased input impedance, while
- magnetic coupling decreases with increased input impedance.

That is, electric fields, E, are a problem with high input impedance, because the induced current results in a high voltage similar to that given by equation (11.51)

$$v = i_c \times R_s \,//\, Z_{in} = C_c \frac{dv}{dt} \times R_s \,//\, Z_{in} \tag{11.51}$$

while magnetic fields, H, are a problem with low input impedance, because the induced voltage results in a high current similar to that given by equation (11.52)

$$i = \frac{v_c}{R_s \,//\, Z_{in}} = \frac{M \dfrac{di}{dt}}{R_s \,//\, Z_{in}} \tag{11.52}$$

In the ***far field*** the r^{-1} term dominates.

In the far field region both the E and H fields are in phase and at right angles. Importantly their magnitudes both decrease, inversely proportionally with distance r, so their magnitude ratio remains constant. That is, in the far field the characteristic impedance $Z_o = E / H = \sqrt{\mu_o / \varepsilon_o} = 120\pi = 377\Omega$ is constant. The far field radiation wave with this constant impedance is termed a *plane wave*. The electric field component of the plane wave tends to dominate interference problems in the far field region.

11.3.1iii - Electric field coupling is caused by changing voltage differences, dv/dt, between conductors. This coupling is usually modelled by capacitance.
The changing electric field produces a current according to $i = C_c\, dv/dt$, where coupling capacitance C_c is dependant on distance of separation, area, and the permittivity of the media. The effect of the produced current is dependant on the source impedance R_s and the effective input impedance, Z_{in}, of the victim equipment as given by equation (11.51).

11.3.1iv - Magnetic field coupling is due to changing currents, di/dt, flowing in conductors. This coupling mechanism is usually modelled by a magnetically coupled circuit, or a transformer, according to $v = M di/dt$, where the resultant current is given by equation (11.52). The mutual inductance M is related to loop area, orientation, separation distance, and screening and its permeability. This induced

voltage is independent of any ground connection or electrical connection between the coupled circuits. Magnetic field problems tend to be at low frequencies. Below 100kHz effective screen materials (due to the skin effect) are steel, mu-metal (μ_r = 20,000), and permalloy, while at higher frequencies the good electrical conduction properties of copper and aluminium are more effective despite there much lower permeabilities.

11.3.2 Mains filters

The conducted ac mains borne noise can be attenuated to safe levels by filtering. The simplest type of filter is an inductor in series with the load in order to reduce any current *di/dt* changes. It is usual practice to use *L-C* filtering, which gives second-order attenuation. The typical circuit diagram of an ac mains voltage filter, with common mode noise filtering, is shown in figure 11.11c. The core inductance is only presented to any ampere-turn imbalance (common mode current), not the much larger principle throughput (go and return) ac current, hence the core dimensional requirements can be modest. Extra non-coupled inductance is needed for differential mode filtering, as shown in figure 11.11d. Only the higher frequency noise components can be effectively attenuated since the filter must not attenuate the 50/60 Hz ac mains component.

11.3.3 Noise filtering precautions

For power electronics, circuit noise suppression and interaction is ultimately based on a try-it and see approach. Logic and experience do not necessarily prevail. The noise reduction precautions to follow are orientated towards power electronics applications.
Good circuit layout and construction (incorporated at the initial design stage) can greatly reduce the radiated noise, both transmitted and received. Obvious starting points are minimising wire loop lengths, using ground planes, capacitor decoupling, twisted wire pairs, and judicious placement of magnetic components. Use opto-couplers, not only to isolate signals but to allow flexible signal grounding that can bypass ground power noise around sensitive circuitry. Sensitive electronic circuitry should be rfi radiation protected by copper (electric and high frequency magnetic) or mild steel (low frequency magnetic) sheeting, depending on the type of radiation and frequency. Shielding, including electrically isolated heatsinks, should be electrically connected to a point that minimises interference. This may involve connection to supply rails (one of positive, zero, negative) or ground.
An *R-C* snubber across a diode decreases *dv/dt* while a series inductive snubber will limit *di/dt*. Mains ac supply series input inductors for bridge rectifiers (plus diode *R-C* snubbers) decrease the amount of diode recovery noise injected back into the mains and into the equipment. Most effective are common mode transformers in all input and output connection cabling. Although differential mode line inductors may be effective in decoupling input power lines, stability issues can arise when used in output cables. Figure 11.12 outlines the frequency bands where the various interference modes can be expected, and the techniques commonly used to suppression that interference.

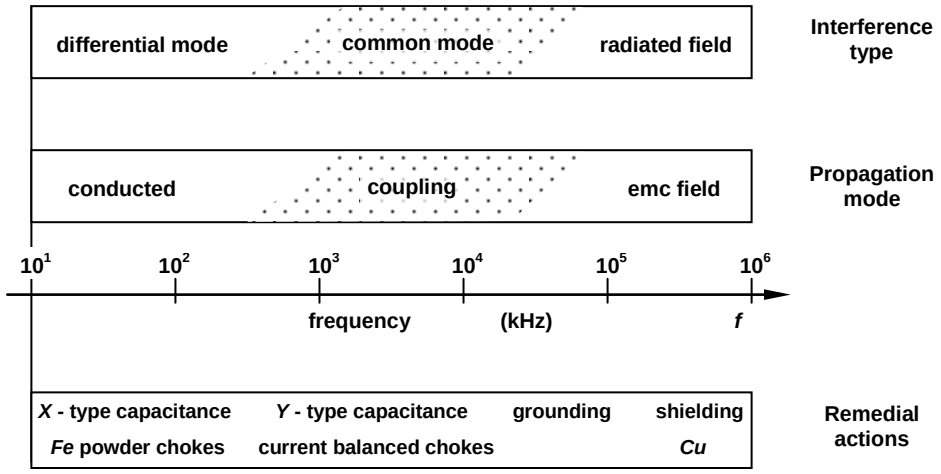


Figure 11.12. *Expected interference types, mode of propagation, and remedial techniques depending on the interference frequency.*

In ac circuit applications, zero-voltage turn-on and zero-current turn-off minimise any rapid changes in current, thus reducing radiation. To minimise freewheel diode recovery noise, slow down switch turn-on.
To minimise interactive noise effects, high noise immune circuit designs can be employed which utilise mos technology. The high-voltage input thresholds of cmos logic (4000 series), 74AC (not ACT) logic

series, and power MOSFETs and IGBTs (high gate threshold and capacitance), offer circuit noise immunity. Gates with Schmitt trigger (hysteresis) inputs are preferable, for example, 4093, 74AC132, etc. Since noise possesses both magnitude and duration, the much slower response times (along with high input thresholds) of 4000 HEF series cmos (or HEF series for a wider operating temperature range) may result in better noise immunity in applications requiring clock frequencies below a few megahertz.
DSP core operating voltages below a few volts necessitate: the use of multilayer pcbs with ground planes, carefully layout separating analogue and digital circuitry (& grounding), low inductance ceramic chip decoupling, watchdog circuitry, etc. Do not avoid using analogue circuitry (±12V), if it is applicable.

11.4 Earthing

The planet earth is electrically neutral. This means that it has the same number of electrons and protons, so their charges cancel out overall. Thus the earth has an electric potential of zero. The earth wire of a mains plug is connected to the actual earth, terra firma (Terre/French, terra/Latin for earth). Because of the size of the earth it is not possible to charge up anything wired to earth.

This inability to charge equipment connected to the earth is the reason that many systems have their metal boxes wired electrically to the earth. This means that any fault inside the equipment cannot produce a dangerous voltage on its enclosing metal box, so no electric shock is possible from touching the outside of the box even if internally there is an electrical fault.
Copper is one of the better and commonly used materials for earth electrodes and underground conductors, especially for a buried earth electrode.
The reasons for having an earthed system are:

- To provide a sufficiently low impedance to facilitate satisfactory protection operation under fault conditions.
- To ensure that living beings in the vicinity of substations are not exposed to unsafe potentials under steady state or fault conditions.
- To retain system voltages within reasonable limits under fault conditions (such as lightning, switching surges or inadvertent contact with higher voltage systems), and ensure that insulation breakdown voltages are not exceeded.
- Custom and practice.
- Graded insulation can be used in power transformers.
- To limit the voltage to earth on conductive materials which enclose electrical conductors or equipment.
- To stabilise the phase to earth voltages on electricity lines under steady state conditions, e.g. by dissipating electrostatic charges which have built up due to clouds, dust, sleet, etc.
- A means of monitoring the insulation of the power delivery system.
- To eliminate persistent arcing ground faults.
- To ensure that a fault which develops between the high and low voltage windings of a transformer can be dealt with by primary protection.
- To provide an alternative path for induced current and thereby minimise the electrical “noise” in cables.
- Provide an equipotential platform on which electronic equipment can operate.

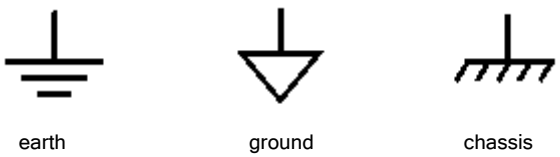


Figure 11.13. *Three different grounding symbols.*

As shown in figure 11.13, various symbols are used on circuit diagrams to represent earth or ground potential. It is usually assumed that they all mean ‘zero volts’, that is, the place from which all other voltages in the circuit are referenced or measured. In practice, the meanings of the symbols are slightly different, specifically:

- The earth symbol indicates a place actually wired to terra firma via the mains wires provided or using a wire to a non-corroding metal plate buried in the earth.
- The ground symbol usually indicates a connection back to a place in the power supply, which provides the energy required by the circuit in order to work. It is usually assumed that this place in the power supply is connected to the earth.

- The chassis symbol means a connection to a metal box enclosing the circuit. As far as the circuit is concerned, this metal box is as good a place as the earth for referencing voltages. From the point of view of most electronic circuits, this functions just like an earth connection, however it need not actually be connected to the earth. Hence the chassis of some equipment can potentially be charged up to a high voltage, with respect to the earth.

In most cases, the ground and chassis connections are just indirect paths to earth. However, in some cases, for example, a portable radio using batteries, or the electrics in a vehicle, the ground or chassis represent a sort of 'local' or 'floating' version of the earth used as the zero volts reference point. In most vehicles, the electrical equipment is powered from a 12(/24)V battery. This provides 12V (positive or negative) with respect to the metal bodywork (the chassis). So far as all the vehicle electronics is concerned, it experiences only 12V. However this does not prevent an electric shock when stepping in or out of the vehicle. This is because the chassis may sometimes become charged up to a high voltage with respect to the earth due to movement of the insulating rubber tyres.

There are several factors which influence or determine the size required for a circuit protective conductor. A minimum cross-sectional area of 2.5mm^2 copper is required for any separate circuit protective conductor, that is, one which is not part of a cable or formed by a wiring enclosure or contained in such an enclosure.
An example would be a bare or insulated copper conductor clipped to a surface, run on a cable tray or fixed to the outside of a wiring enclosure. Such a circuit protective conductor must also be suitably protected if it is liable to suffer mechanical damage or chemical deterioration or be damaged by electrodynamic effects produced by passing earth fault current through it. If mechanical protection is not provided the minimum size is 4mm^2 copper or equivalent.
There are two methods for sizing protective conductors including earthing conductors.
The easier method is to determine the protective conductor size from standard tables but this may produce a larger size than is strictly necessary, since it employs a simple relationship to the cross-sectional area of the phase conductor(s).
The second method involves a formula calculation.
The formula is commonly referred to as the *adiabatic equation* and is the same as that used for short-circuit current calculations.
It assumes that no heat is dissipated from the protective conductor during an earth fault and therefore errs on the safe side. Even so, application of the formula will in many instances result in a protective conductor having a smaller cross sectional area than that of the live conductors of the associated circuit. This is quite acceptable.
The nominal cross-sectional area of the conductor in mm^2, *S*, shall be not less than the value given by:

$$S = \sqrt{I^2 t} \,/\, k$$

I is the value in amperes (rms for ac) of the fault current for a fault of negligible impedance, which can flow through the associated protective device, accounting for the current limiting effect of the circuit impedances and the limiting capability (I^2t) of that protective device. Account is taken of the effect, on the resistance of circuit conductors, of their temperature rise as a result of over-current.

t is the operating time of the disconnecting device in seconds corresponding to the fault current I amperes.

k is a factor taking account of the resistivity, temperature coefficient and heat capacity of the conductor material, and the appropriate initial and final temperatures.

11.4.1 Earth and neutral

International standard IEC 60364 distinguishes three categories of earthing arrangements, using the two-letter codes, viz., *TN*, *TT*, and *IT*.

The first letter indicates the connection between earth and the three-phase power-supply equipment generator or transformer:

T: (Latin→French: *terra*): Direct connection of a point with earth;

I: No point is connected with earth (isolated), except perhaps via a high impedance.

The second letter indicates the connection between earth and the electrical device being supplied:

T: Direct connection of a point with earth

N: Direct connection to neutral at the origin of installation, which is connected to the earth

The remaining letter:

C: Combined neutral and protective earth functions (same conductor).

S: Separate neutral and protective earth functions (separate conductors).

1. *TN* networks

In a ***TN*** earthing system in Table 11.1, one of the points in the generator or transformer is connected with earth, usually the star point in a three-phase system. The body of the electrical device is connected with earth via this earth connection at the transformer.

The conductor that connects the exposed metallic parts of the consumer's electrical installation is called *protective earth* (*PE*: *Ground*). The conductor that connects to the star point in a three-phase system, or that carries the return current in a single-phase system, is called *neutral, N*.

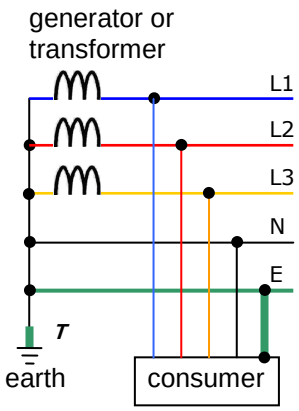
Three variants of ***TN*** systems are:

i. ***TN−S***:- Conductors *PE* and *N* are separate and are connected together only near the power source. That is the supplier provides a separate earth conductor back to the substation. This is most commonly done by having an earthing clamp connected to the sheath of the supply cable. This arrangement is the current standard for most residential and industrial electric systems in North America and Europe.

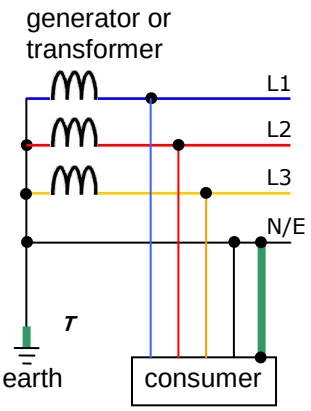
ii. ***TN−C***:- No separate earth conductors exist anywhere. A combined *PEN* conductor fulfils the functions of both a *PE* and an *N* conductor. Rarely used scheme.

iii. ***TN−C−S***:- Part of the system uses a combined *PEN* conductor, which is at some point split into separate *PE* and *N* lines. The combined *PEN* conductor typically occurs between the substation and the entry point into the building, and separated in the service head. The earthing conductor is connected to the supplier's neutral. In the UK, this system is also known as protective multiple earthing (*PME*), because of the practice of connecting the combined neutral-and-earth conductor to real earth at many locations, to reduce the risk of broken neutrals - with a similar system in Australia being designated as multiple earthed neutral (*MEN*).

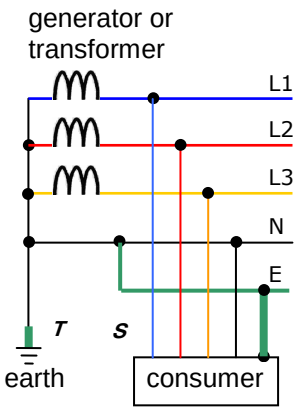
Table 11.1 Neutral/earth systems



TN-S:
Separate protective earth (*PE*) and neutral (*N*) conductors from the transformer to the consuming device, not connected together at any point after the building distribution point.



TN-C:
Combined *PE* and *N* conductor all the way from the transformer to the consuming device.



TN-C-S:
Combined *PEN* conductor from the transformer to the building distribution point, but separate *PE* and *N* conductors in fixed indoor wiring and flexible power cords.

It is possible to have both *TN-S* and *TN-C-S* supplies from the same transformer. For example, the sheaths on some underground cables corrode and stop providing good earth connections, so homes with *bad earths* are converted to *TN-C-S*.

2. *TT* network

In a ***TT*** earthing system, in figure 11.14a, the protective earth connection of the consumer is provided by a local connection to earth, independent of any earth connection at the generator. No earth is provided by the supplier; the installation requires its own (one or more) earth rod (common used with overhead supply lines).

The advantage of the *TT* earthing system is that it is clear of high and low frequency noises that come through the neutral conductor from the connected equipment. *TT* is preferred for special applications like telecommunication sites that benefit from interference-free earthing. Also, *TT* does not have the risk of a broken neutral.

In locations where power is distributed overhead and *TT* is used, installation earth conductors are not at risk should any overhead distribution conductor be fractured by, say, storm damage.

Before RCDs, the *TT* earthing system was unattractive for general use because of its poor capability of accepting high currents in the case of a live-to-*PE* short circuit (compared to *TN* systems). The *TT* earthing system is attractive for premises where all AC power circuits are RCD-protected.

The *TT* earthing system is used throughout Japan, with RCD units in most industrial settings. This can impose added requirements on variable frequency drives and switched-mode power supplies which often have substantial filters passing high frequency noise into the ground conductor.

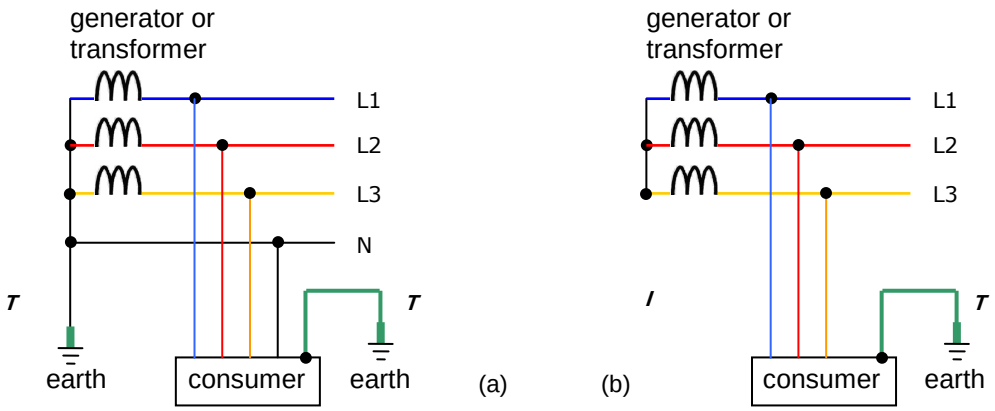


Figure 11.14. *Earth/neutral systems: (a) TT network and (b) IT network.*

3. *IT* network

In an ***IT*** network, in figure 11.14b, the electrical distribution system has no connection to earth, or it has only a high impedance connection. In such systems, an insulation monitoring device is used to monitor the impedance. The supply may be embedded generation or a portable generator with no earth connection, so the installation has its own earth rod.

NB. House grounding is normally established by connecting (clamping) the household earth system wire to a metal gas/water pipe (stake-less). Although this connection may appear satisfactory, much unseen piping once underground may be made of plastic – an insulator.

11.5 Isolation (galvanic)

Incorporating isolation, both electrically and physically, into a system has many functions: preventing ground loops (11.3.3) – including static and dynamic channel cross talk, rejecting common-mode voltage – noise reduction (11.3.1), allowing two circuits to operate at different reference voltage levels (level shifting), protecting equipment from surges, lightening strikes, etc., and providing electrical safety (11.4). Wireless type techniques are mainly reserved for remote monitoring involving low band width temperature, vibration, deflection, speed, etc. type measurements. Isolation where the ground wire is passes through the system, as with transformers or a misconception with UPS, are not considered.

Difference between ***isolation*** and ***insulation***

In terms of power electronics, isolation refers to systems that do not share a common electrical reference or ground. The level of isolation is insulation which is a measure of the impedance (related to voltage breakdown) separation between systems not sharing a common ground. For example, a switch isolates a light bulb from the ac mains, but the switch air gap has a voltage insulation breakdown level. The same reasoning can be applied to a transformer - the primary and secondary are physical isolated (separated), but the two windings have an interwinding insulation voltage break down level due to the enamel coating, physical construction, etc. IGBTs are available in modules with an insulated ceramic base plate arrangement, but have an isolation test voltage rating.

11.5.1 Isolation problem and related measurements

i *Ground Loops*

Ground loops a common source of noise in power electronics applications. They occur when two connected terminals in a circuit are at different ground potentials, causing current to flow between the two terminals. The local system ground can be several volts above or below the ground of the other system, and nearby lightning strikes can cause the difference to rise to several hundreds or thousands of volts. This additional voltage can cause significant error in the measurement (notwithstanding a catastrophic fault), but the current that causes it can also couple voltages in nearby connections. These voltage errors can appear as transients or periodic signals. For example, if a ground loop is formed with 50/60Hz AC power lines, the unwanted AC signal appears as a periodic voltage error in a measurement.

When a ground loop exists, the measured voltage, V_m, in figure 11,15 is the sum of the signal voltage, V_s, and the potential difference, ΔV_g, which exists between the signal source ground and the measurement system ground (as shown in Figure 11.15). This potential is generally not a DC level; thus, the result is a noisy measurement system often showing power-line frequency (50/60 Hz) components in the readings.

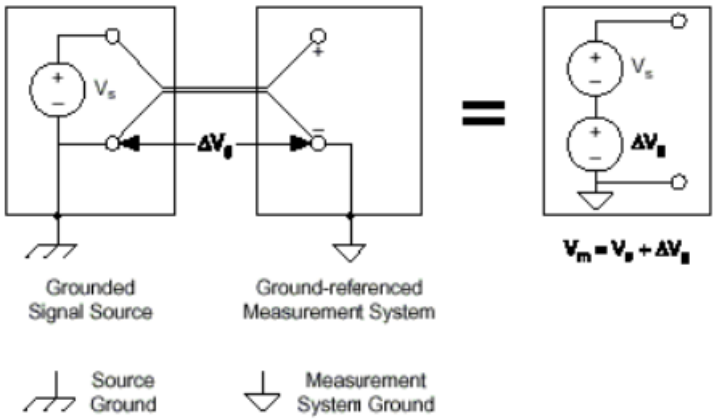


Fig. 11.15 *Ground loop noise.*

To avoid ground loops, ensure that there is only one ground reference in the measurement system, or use isolated instrumentation. Using isolated hardware near eliminates the path between the ground of the source and the secondary circuit, be it a measurement device or circuit, thus preventing any current from flowing between multiple ground points.

ii *Common-mode Voltage*

An ideal differential measurement system responds only to the potential difference between the two op amp terminals, the +ve and -ve inputs. The differential voltage across the circuit pair is the desired signal, yet an unwanted signal may exist that is common to both sides of a differential circuit pair. This voltage is known as common-mode voltage. An ideal differential measurement system will reject, rather than measure, the common-mode voltage. Practical devices, however, have several limitations, such as common-mode voltage range and common-mode rejection ratio (CMRR), which limit this ability to reject the common-mode voltage.

The *common-mode voltage range* is defined as the maximum allowable voltage swing on each input with respect to the measurement system ground. Violating this constraint results not only in measurement error, but also in possible system damage.

Common mode rejection ratio is the ability of a measurement system to reject common-mode voltages. Amplifiers (or an electronic circuit)) with a higher common-mode rejection ratio is more effective at rejecting common-mode voltages. The common-mode rejection ratio (CMRR) is shown graphically in Figure 11.16 and is defined as the logarithmic ratio of differential gain to common mode gain, viz.:

$$CMRR\ (dB) = 20\ \log \frac{Differential\ Gain}{Common-Mode\ Gain} \tag{11.53}$$

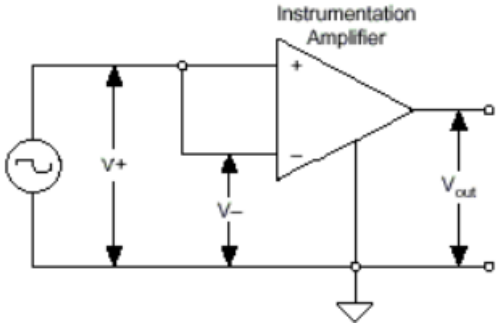


Fig. 11.16 *Common mode voltage rejection.*

In a non-isolated differential measurement system, an electrical path still exists in the circuit between input and output. Therefore, electrical characteristics of the amplifier limit the common mode signal level that can be applied to the input. With the use of isolation amplifiers, the conductive electrical path is eliminated and the common-mode rejection ratio is increased.

11.5.2 Isolation mechanisms

Physical isolation, a basic form of isolation, is where there is a physical barrier (air, vacuum, insulator, or any non-conductive material) between two electrical systems. With pure physical isolation, no signal transfer exists between electrical systems. With isolated electrical systems, transfer, or coupling, of energy across the isolation barrier is required.

There are three basic types of electrical isolation that can be used, in power electronic, signal and data acquisition systems:

i ***Optical Isolation*** *(figure 11.17)*
Optical isolation is common in digital isolation systems. The media for transmitting the signal is light and the physical isolation barrier, typically an air gap. The light intensity is proportional to the measured signal. The light signal from a photo diode is transmitted across the isolation barrier and detected by a photoconductive element on the other side of the isolation barrier.

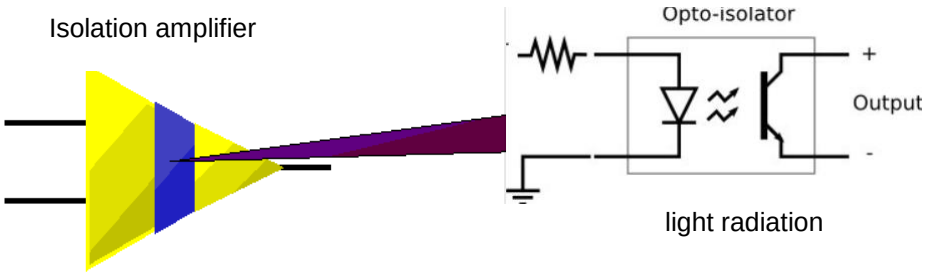


Figure 11.17. *Optocoupling.*

ii ***Electromagnetic Isolation*** *(figure 11.18)*
Electromagnetic isolation uses a transformer to couple a signal across an isolation barrier by generating an electromagnetic field proportional to the electrical signal. The field is created and detected by a coupled pair of conductive coils. The physical barrier can be air or another non-conductive barrier.

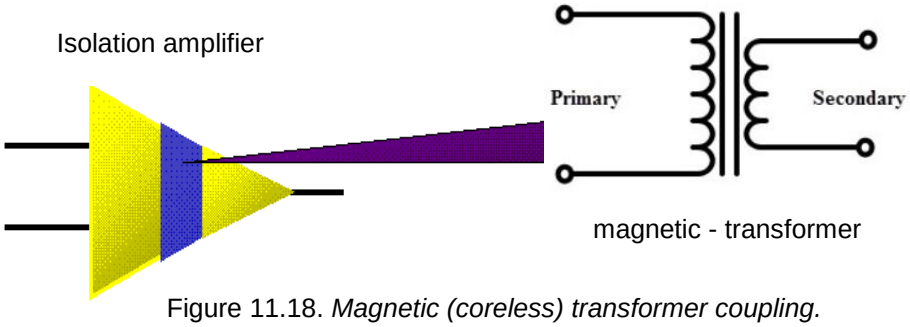


Figure 11.18. *Magnetic (coreless) transformer coupling.*

iii ***Capacitive Isolation*** *(figure 11.19)*
With capacitive isolation, an electromagnetic field changes the level of charge on the capacitor. This charge is detected across the barrier and is proportional to the level of the measured signal.

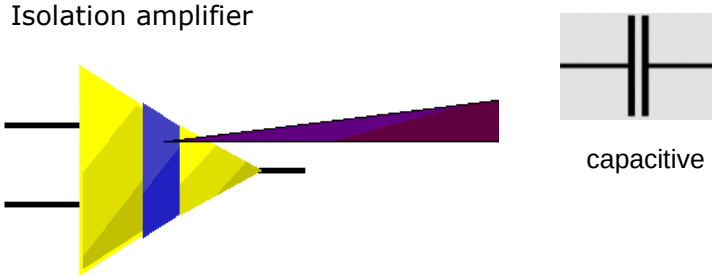


Figure 11.19. *Capacitive isolation.*

Reading list

Grafham, D.R. *et al., SCR Manual,*
General Electric Company, 6th Edition, 1979.

Williams, T., *EMC for Product Designers*,
Newnes, 2nd Edition, 1998.

Problems

11.1. Derive an expression for the worst case maximum allowable voltage-sharing resistance for n series devices each of voltage rating V_D and maximum leakage I_m across a supply V_s. The resistance tolerance is ± 100a per cent and the supply tolerance is ± 100b per cent.
If V_s = 1500 V, V_D = 200 V, I_m = 10 mA, n = 10 and tolerances are ±10 per cent, calculate resistance and maximum total power losses if
i. tolerances are neglected
ii. only one tolerance is considered
iii. both tolerances are included.
[i. R <5.5 kΩ, 63.8 W; ii. R <2.1 kΩ, 185 W; R <3.9 kΩ, 91 W; iii. R <280 Ω, 1234 W].

11.2. Derive a power loss expression for a voltage-sharing resistance network in which both supply and resistance tolerances are included. Assume a dc reverse bias of duty cycle δ.

11.3. Derive the power loss expression for an SCR string with voltage-sharing resistance and an ac supply.

11.4. Two diodes modelled as in figure 2.4a having characteristics approximated in the forward direction by
Diode D_1: $V_F = 1.0 + 0.01\ I_F$ (V)
Diode D_2: $V_F = 0.95 + 0.011\ I_F$ (V)
are connected in parallel. Derive general expressions for the voltage across and the current in each diode if the total current is 200 A.
At what total current and voltage will the diodes equally share?
[102.4 A, 97.6 A, 2.02 V; 100 A, 1.5 V]

11.5. In problem 11.4, what single value of resistance in series with each parallel connected diode match the currents to within 1 per cent of equal sharing? Calculate the resistor maximum power loss.
How will the current share at I_T = 100 A and I_T = 500A with the balancing resistors.
[14.5 mΩ, 148 W; 50 A, 50 A; 254 A, 246 A]

11.6. A Zener diode has an I-V characteristic described by $I = kV^{30}$. What percentage increase in voltage will increase the power dissipation by a factor of 1000?
[25 per cent]

11.7. What is the percentage decrease in the dynamic resistance of the Zener diode in question 11.6?
[99.845 per cent]

11.8. A string of three 2,600 V thyristors connected in series is designed to withstand an off-state voltage of 7.2 kV. If the compensating circuit consists of a series 33 Ω, 0.01 μF snubber in parallel with a 24 kΩ resistor, across each thyristor, and the leakage currents for the thyristors are 20 mA, 25 mA, and 15 mA, at 125°C, calculate the voltage across each thyristor, then the discharge current of each capacitor at turn-on.
[2400 V, 2280 V, 2520 V, 72.73 A, 69.09 A, 76.36 A]

11.9. The reverse leakage current characteristics of two series connected diodes are
Diode D_1: $I_1 = -10^{-4} V_1 + 0.14$ (A) for $V_1 < -1400$ V
Diode D_2: $I_2 = -10^{-4} V_2 + 0.16$ (A) for $V_2 < -1600$V
If the resistance across diode D_1 is 100 kΩ and $V_{D1} = V_{D2} = -2000$ V, what is the leakage current in each diode and what resistance is required across diode D_2?
[0.34 mA, 0.36 mA, ∞]

11.10. Two high voltage diodes are connected in series as shown in figure 11.5a. The dc input voltage is 5 kV and 10 kΩ dc sharing resistors are used. If the reverse leakage current of each diode is 25mA and 75mA respectively, determine the voltage across each diode and the resistor power loss.
[2750 V, 2250 V, 756.25 W, 506.25 W]

11.11. The forward characteristics of two parallel connected diodes are
Diode D_1: $I_1 = 200 V_1 - 100$ (A) for $V_1 \geq 0.5$ V
Diode D_2: $I_2 = 200 V_2 - 200$ (A) for $V_2 \geq 1$V
If the forward voltage of the parallel combination is 1.5V, determine the forward current through each diode.
[200 A, 100 A]

11.12 Two diodes are connected in parallel and with current sharing resistances as shown in figure 11.7. The forward I-V characteristics are as given in problem 11.11. The voltage across the parallel combination is 2V and the balancing resistors are equal in value.
Calculate each diode voltage and current. Calculate resistor maximum power loss. Let $I_{tot} = 400$A.

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